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(54) Driving apparatus and method for a plasma display panel

(57) A driving apparatus comprises switches SW1 to Sw3, a first signal line OUTA, and a second signal line OUTB. By ON/OFF control of the switches SW1 to Sw3, the voltage of the first signal line OUTA is changed between a positive voltage (+1/2V) level, which is smaller than a voltage V to be applied to a load 20, and the ground level, and the voltage of the second signal line OUTB is changed between the ground level and a negative voltage (-1/2V). By ON/OFF control of switches SW4 and SW5, the positive and negative voltages given by the first and second signal lines are selectively applied to the load 20. The maximum voltage applied to each element in the driving apparatus can be thereby lowered to the voltage (1/2V), which is smaller than the voltage V to be applied to the load 20. This makes it possible to hold down the breakdown voltage of each element to half the value in previously-considered apparatus.

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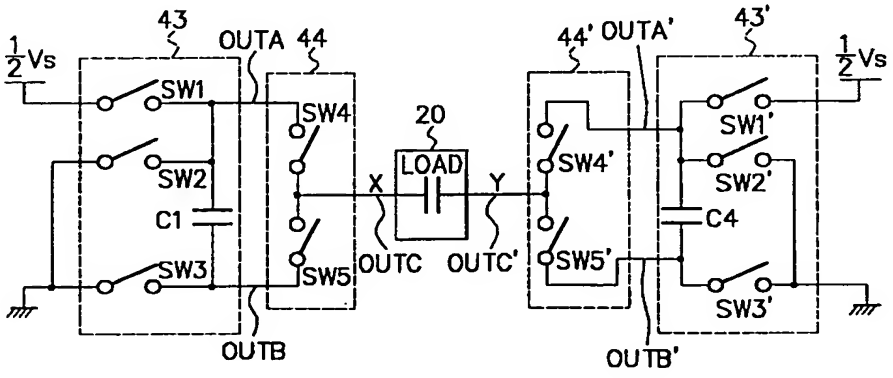

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The voltage by wall charges themselves then exceeds the discharge start voltage in every cell, and discharge starts. This discharge makes no wall charge because there is no difference in potential between electrodes. Space charges are neutralized by themselves to end discharge. This is so-called self-erase discharge. By this self-erase discharge, all cells in the panel become a uniform state free from wall charges. This reset period serves to set all cells in the same state independently of the ON/OFF state of each cell in the preceding subfield. This makes it possible to perform the subsequent address (write) discharge stably.

[0015] Next, in the address period, address discharge is line-sequentially performed to turn each cell ON/OFF in accordance with display data. More specifically, a voltage at -Vy level (about -150 V) is applied to the scanning electrode Y1 corresponding to the first display line, and a voltage at -Vsc level (about -50 V) is applied to the scanning electrodes Y2 to Yn corresponding to the remaining display lines. At the same time, an address pulse having a voltage Va (about 50 V) is selectively applied to an address electrode Aj corresponding to a cell to undergo sustain discharge, i.e., to be turned ON, in the address electrodes A1 to Am.

[0016] Consequently, discharge occurs between the scanning electrode Y1 and the address electrode Aj of the cell to be turned ON. With this priming (pilot), discharge between the scanning electrode Y1 and the corresponding common electrode X having a voltage Vx starts immediately. An amount of wall charges enough for the next sustain discharge is then stored on the surface of the MgO protective film 13 on the common electrode X and the scanning electrode Y1 of the selected cell. Similarly for the scanning electrodes Y2 to Yn corresponding to the remaining display lines, the voltage at -Vy level is applied to the scanning electrodes of selected cells in order, and the voltage at -Vsc level is applied to the remaining scanning electrodes of non-selected cells. New display data is thereby written in all display lines.

[0017] In the subsequent sustain discharge period, a sustain pulse having the voltage Vs (about 200 V) is alternately applied to the scanning electrodes Y1 to Yn and the common electrodes X to perform sustain discharge. An image of one subfield is displayed. The luminance of the image is determined by the length of the sustain discharge period, i.e., the number of times or the frequency of sustain pulse application.

[0018] In such an AC-driven PDP, the voltage Vf at which a gas discharge starts between the surfaces of the common and scanning electrodes X and Y, is within the range of 220 to 260 V in general. Within an address period, e.g., in a cell to display, the voltage is applied between the address and scanning electrodes A and Y to make a gas discharge occur. Using it as a trigger, a discharge is made to occur between the common and scanning electrodes X and Y, so as to leave wall charges on the common and scanning electrodes X and Y in the cell.

[0019] In the subsequent sustain discharge period, with the wall charges Vwall generated in the address period, and the sustain pulse voltage Vs applied between the common and scanning electrodes X and Y, a gas discharge can be made to occur by setting $|Vs + Vwall|$ at Vf or more. The value of the voltage Vs is not more than the discharge start voltage Vf. A voltage value that $|Vs| < |Vf| < |Vs + Vwall|$ is used as Vs.

[0020] When a gas discharge once occurs between the common and scanning electrodes X and Y, the wall charges on the common and scanning electrodes X and Y in the cell are replaced by wall charges in the reverse polarity to end the gas discharge. Thus a sustain pulse voltage Vs in the polarity reverse to the previous one is applied between the common and scanning electrodes X and Y. A gas discharge thereby occur again using the wall charges newly generated on the common and scanning electrodes X and Y. By repeating the above operations, the gas discharges can be repeated.

[0021] The above-described "write address method" is an example of driving method for such an AC-driven PDP, in which the wall charges of all cells in the panel are erased in a reset period, and cells to display are selectively subjected to discharges in the subsequent address period to accumulate wall charges. Contrastingly in "erasion address method" as another example, wall charges are accumulated in relation to all cells in the panel in a reset period, and cells not to display are selectively subjected to discharges in the subsequent address period to erase their wall charges, thereby leaving wall charges only in cells to display.

[0022] Fig. 4 is a circuit diagram showing a partial construction of a driving apparatus for the previously-considered PDP apparatus. Referring to Fig. 4, a load 20 represents the total capacitance of the cells formed between one common electrode X and one scanning electrode Y. The load 20 is provided with a common electrode X and a scanning electrode Y, to which pulse voltages described with Fig. 3 are applied by the X-side circuit 2 and the Y-side circuit 3.

[0023] The X-side circuit 2 includes a power supply circuit 21, a power recovery circuit 22, and a sustainer circuit 23. The power supply circuit 21 comprises a diode D1 connected to the power supply line of the sustain pulse voltage Vs, transistors Tr1 and Tr2 connected in series between the ground (GND) and the power supply line of the write voltage Vw, and a capacitor C1, connected between the common drain of the transistors Tr1 and Tr2 and the output of the diode D1.

[0024] To apply the full write pulse to the common electrodes X in the reset period, the transistor Tr1 is turned ON, and the transistor Tr2 is turned OFF. The sustain pulse voltage Vs having passed through the diode D1 and the write voltage Vw are summed and supplied to the sustainer circuit 23. To apply the sustain pulse to the common electrodes X in the sustain discharge period, the transistor Tr1 is turned OFF, and the

(= 100 V) between both terminals of the scan driver. Further, the switch SW21 is turned ON to apply a voltage (-Vy = -180 V) to one scanning electrode Y which is the scanning target, and the switch SW20 is turned ON to apply a voltage (Vsc - Vy = - 80 V) to the remaining scanning electrodes Y.

[0040] At the intersection between the scan pulse of - 180 V to the one scanning electrode Y which is the scanning target, and each address electrode A, e.g., in case of making a display, a gas discharge is made to occur by a voltage Va (= 60 V) applied to the address electrode A. Using the gas discharge between the address and scanning electrodes A and Y as a trigger, a discharge is further made to occur between the common electrode X (to which a voltage Vax is applied by turning the switch SW7 ON) and the scanning electrode Y (to which a voltage of -180 V is applied). Wall charges different in polarity from the applied voltages are thereby generated on the dielectric layer 12 on the scanning electrodes X and Y shown in Fig. 2. This operation is performed to every scanning electrode Y.

[0041] The A/S separation circuit is for preventing a short circuit between the diode D1 and the switch SW16 in its ON state due to the voltage (-Vy) that is lower than the ground level, and for preventing a short circuit between the switch SW18 and a diode parasitic on the switch SW11 due to the voltage Vsc that is lower than the ground level. During the above operation, the switch SW15 is kept OFF. A voltage of 180 V is applied between both terminals of the switch SW15.

[0042] In the subsequent sustain discharge period, the switches SW12 and SW15 on the scanning electrode Y side are turned ON, and the switch SW2 on the common electrode X side is turned ON. An L-C resonance thereby occurs by the coil L3 and the capacitance Cp of the PDP panel with using the capacitor C2, whose one terminal is always grounded, as a power supply. The voltage on the scanning electrode Y side is raised near Vs. Next, the switch SW10 is turned ON to raise the voltage to Vs, and thereby the voltage being applied to the scanning electrode Y is set at Vs. At this time, the voltage Vs (= 180 V) is applied between both terminals of the switch SW 11, which is being OFF.

[0043] The voltage Vs being applied between the common and scanning electrodes X and Y is thereby added to a voltage due to wall charges generated in the above-described scanning period, and so a gas discharge starts. The current then flows through the switches SW10, SW15, and SW2. At this time, wall charges are again generated as described above.

[0044] Next, on the scanning electrode Y side, the switches SW10 and SW12 are turned OFF, and the switch SW13 is turned ON. An L-C resonance thereby occurs by the coil L4 and the capacitance Cp of the PDP panel with using the capacitor C2, whose one terminal is always grounded, as a power supply. The voltage on the scanning electrode Y side is lowered near the ground level. Next, the switch SW11 is turned ON to lower the voltage to the ground level, and thereby the voltage being applied to the scanning electrode Y is set at the ground level. At this time, the voltage Vs (= 180 V) is applied between both terminals of the switch SW 10, which is being OFF.

[0045] Next, the switch SW3 on the common electrode X side is turned ON. An L-C resonance thereby occurs by the coil L1 and the capacitance Cp of the PDP panel with using the capacitor C1, whose one terminal is always grounded, as a power supply. The voltage on the common electrode X side is raised near Vs. Next, the switch SW1 is turned ON to raise the voltage to Vs, and thereby the voltage being applied to the common electrode X is set at Vs. At this time, the voltage Vs (= 180 V) is applied between both terminals of the switch SW 2, which is being OFF.

[0046] The voltage Vs being applied between the common and scanning electrodes X and Y is thereby added to a voltage due to wall charges generated some time ago, and so a gas discharge starts. The current then flows through the switches SW1 and SW11. At this time, wall charges are again generated as described above.

[0047] Next, on the common electrode X side, the switches SW1 and SW3 are turned OFF, and the switch SW6 is turned ON. An L-C resonance thereby occurs by the coil L2 and the capacitance Cp of the PDP panel with using the capacitor C1, whose one terminal is always grounded, as a power supply. The voltage on the common electrode X side is lowered near the ground level. Next, the switch SW2 is turned ON to lower the voltage to the ground level, and thereby the voltage being applied to the common electrode X is set at the ground level. At this time, the voltage Vs (= 180 V) is applied between both terminals of each of the switch SW 1 on the common electrode X side and the switch SW10 on the scanning electrode Y side, which are being OFF.

[0048] The breakdown voltages of various elements of the driving apparatus are determined by the maximum voltage of the pulse to be applied to the elements. In the previously-considered driving apparatus, a fixed voltage supplied from the power supply lines is applied to the load. For example, one of the X and Y electrodes is set at the ground level and the fixed voltage is applied to the other. For this reason, each element in the driving apparatus must have a high breakdown voltage corresponding to the fixed voltage.

[0049] In particular, in case of the construction shown in Fig. 4, each element making up the sustainer circuit 23 in the X-side circuit 2, requires a very high breakdown voltage corresponding to the full write pulse voltage Vs + Vw (about 400 V). Thus an expensive and large switching element such as a FET must be used to ensure a sufficient breakdown voltage. This causes a complex circuit construction and a very high manufacturing cost.

[0050] Besides, in case of the construction shown in Fig. 5, the breakdown voltage of each FET of the switch-

ing waveforms of pulse voltages applied to electrodes X and Y in a sustain discharge period;
Fig. 17 is a chart showing another example of driving waveforms of pulse voltages applied to electrodes X and Y in a sustain discharge period;
Fig. 18 is a chart showing another example of driving waveforms of pulse voltages applied to electrodes X and Y in a sustain discharge period;
Fig. 19 is a chart showing another example of driving waveforms of pulse voltages applied to electrodes X and Y in a sustain discharge period;
Fig. 20 is a chart showing another example of driving waveforms of pulse voltages applied to electrodes X and Y in a sustain discharge period;
Fig. 21 is a timing chart showing an example of switching control for generating the waveforms shown in Fig. 14;
Fig. 22 is a timing chart showing an example of switching control for generating the waveforms shown in Fig. 15;
Fig. 23 is a timing chart showing an example of switching control for generating the waveforms shown in Fig. 16;
Fig. 24 is a timing chart showing an example of switching control for generating the waveforms shown in Fig. 17;
Fig. 25 is a timing chart showing an example of switching control for generating the waveforms shown in Fig. 18;
Fig. 26 is a timing chart showing another example of switching control for generating the waveforms shown in Fig. 19;
Fig. 27 is a timing chart showing an example of switching control for generating the waveforms shown in Fig. 20;
Fig. 28 is a timing chart showing another example of switching control for generating the waveforms shown in Fig. 21;
Fig. 29 is a timing chart showing an example of switching control for generating the waveforms shown in Fig. 22;
Fig. 30 is a circuit diagram showing another example of construction of a driving apparatus according to the first embodiment;
Fig. 31 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 30;
Fig. 32 is a timing chart showing another example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 30;
Fig. 33 is a circuit diagram showing an example of construction of a driving apparatus according to the second embodiment of the present invention;
Fig. 34 is a circuit diagram showing another example of construction of a driving apparatus according to the second embodiment;
Fig. 35 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 34;
Fig. 36 is a circuit diagram showing an example of construction of a driving apparatus according to the third embodiment of the present invention;
Fig. 37 is a circuit diagram showing another example of construction of a driving apparatus according to the third embodiment;
Fig. 38 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 37;
Fig. 39 is a circuit diagram showing an example of construction of a driving apparatus according to the fourth embodiment of the present invention;
Fig. 40 is a circuit diagram showing another example of construction of a driving apparatus according to the fourth embodiment;
Fig. 41 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 40;
Fig. 42 is a circuit diagram showing an example of construction of a driving apparatus according to the fifth embodiment of the present invention;
Fig. 43 is a timing chart showing an example of driving waveforms in a reset period and the subsequent sustain discharge period by the driving apparatus constructed as in Fig. 42;
Fig. 44 is a circuit diagram showing another example of construction of a driving apparatus according to the fifth embodiment;
Fig. 45 is a timing chart showing an example of driving waveforms by the driving apparatus constructed as in Fig. 44;
Fig. 46 is a circuit diagram showing another example of construction of a driving apparatus according to the fifth embodiment;
Fig. 47 is a timing chart showing an example of driving waveforms in a reset period and the subsequent sustain discharge period by the driving apparatus constructed as in Fig. 46;
Fig. 48 is a circuit diagram showing an example of construction of a driving apparatus according to the sixth embodiment of the present invention;
Fig. 49 is a timing chart showing an example of driving waveforms by the driving apparatus constructed as in Fig. 48;
Fig. 50 is a timing chart showing a manner of power recovery by the power recovery circuit shown in Fig. 48;
Fig. 51 is a circuit diagram showing another example of construction of a driving apparatus according to the sixth embodiment;
Fig. 52 is a timing chart showing the manner of power recovery by the power recovery circuit shown in Fig. 51;
Fig. 53 is a circuit diagram showing another example of construction of a driving apparatus according to the sixth embodiment;
Fig. 54 is a circuit diagram showing another exam-

Fig. 93 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 92;
Fig. 94 is a circuit diagram showing another example of construction of a driving apparatus according to the thirteenth embodiment;
Fig. 95 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 94;
Fig. 96 is a circuit diagram showing another example of construction of a driving apparatus according to the thirteenth embodiment;
Fig. 97 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 96;
Fig. 98 is a circuit diagram showing another example of construction of a driving apparatus according to the thirteenth embodiment;
Fig. 99 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 98;
Fig. 100 is a diagrammatic view showing a schematic construction of a PDP according to the fourteenth embodiment of the present invention;
Fig. 101 is a block diagram showing an example of a schematic construction of a plasma display apparatus according to the fourteenth embodiment;
Fig. 102 is a block diagram showing an example of construction of a driving apparatus according to the fourteenth embodiment;
Fig. 103 is a block diagram showing an example of construction of a driving apparatus according to the fifteenth embodiment;
Fig. 104 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 103; and
Fig. 105 is a circuit diagram showing an example of construction according to still another embodiment.

[0058] Hereinafter, embodiments of the present invention will be described with reference to drawings.

[0059] In this description, use of the term "conventional" does not necessarily imply that the thing referred to is in the public domain, merely that it has been previously considered.

[0060] Fig. 8 is a circuit diagram showing the construction of a driving apparatus according to an embodiment of the present invention.

[0061] The driving apparatus of this embodiment shown in Fig. 8 can be applied to a display panel such as an AC-driven PDP apparatus, though it is not limited to such an application. In this case, the whole construction and the structure in section of each cell are the same as those shown in Figs. 1 and 2.

[0062] Referring to Fig. 8, an A/D converter 42 A/D-converts an AC power supply voltage supplied from an AC power supply 41 to generate a DC power supply voltage. At this time, the A/D converter 42 generates, e.g., a voltage (Vs/2), which is half of a sustain pulse voltage Vs.

[0063] Using the voltage (Vs/2) supplied from the A/D converter 42, a power supply circuit 43 selectively outputs positive and negative voltages (+Vs/2 and -Vs/2). A driver circuit 44 applies, to a load 20, the power supply voltage (±Vs/2) supplied from the power supply circuit 43.

[0064] The power supply circuit 43 and the driver circuit 44 are connected to each other through first and second signal lines OUTA and OUTB. These power supply circuit 43 and driver circuit 44 are connected to the common electrode X side of the load 20 corresponding to the PDP, and make up an X-side circuit 2 shown in Fig. 1.

[0065] A power supply circuit 43' and a driver circuit 44' include the same constructions as the power supply circuit 43 and the driver circuit 44, respectively. The power supply circuit 43' and the driver circuit 44' are connected to each other through third and fourth signal lines OUTA' and OUTB'. These power supply circuit 43' and driver circuit 44' are connected to the scanning electrode Y side of the load 20, and make up a Y-side circuit 3 shown in Fig. 1.

[0066] In this embodiment, the power supply voltage (Vs/2) output from the A/D converter 42 and the ground voltage are supplied to both the power supply circuit 43 for the common electrode X and the power supply circuit 43' for the scanning electrode Y. That is, one A/D converter 42 is shared by the two power supply circuits 43 and 43'.

[0067] Operations of the driving apparatus having the above construction will be described below. For example, in a sustain discharge period, the power supply circuit 43 for common electrode X outputs alternating voltages (+Vs/2, 0) to the first signal line OUTA, and alternating voltages (0, -Vs/2) to the second signal line OUTB. At this time, the power supply circuit 43' for scanning electrode Y outputs alternating voltages (0, +Vs/2) to the third signal line OUTA', and alternating voltages (-Vs/2, 0) to the fourth signal line OUTB' in the reverse phases to those of the power supply circuit 43 for common electrode X.

[0068] The driver circuit 44 for common electrode X outputs the voltages output on the first and second signal lines OUTA and OUTB, onto the output line OUTC to apply them to the load 20. The driver circuit 44' for scanning electrode Y applies the voltages output on the third and fourth signal lines OUTA' and OUTB', to the load 20 through the output line OUTC'.

[0069] In this manner, when the voltage (+Vs/2) of the first signal line OUTA is applied through the output line OUTC to the common electrode X of the load 20, the voltage (-Vs/2) of the fourth signal line OUTB' is applied through the output line OUTC' to its scanning electrode Y. Conversely, when the voltage (-Vs/2) of the second signal line OUTB is applied through the output line

are turned ON to connect the capacitor C1 to the power supply, charges corresponding to the voltage (Vs/2) given through the A/D converter 42 via the switch SW1 are stored in the capacitor C1.

[0083] At the next timing, the switch SW4 is turned OFF to stop the current path for applying the voltage, and then the switch SW5 is turned ON like a pulse. The voltage of the output line OUTC is thereby lowered to the ground level. Next, the switch SW2 is turned ON, and the remaining four switches SW1, SW3, SW4, and SW5 are set OFF. The switch SW4 is then turned ON like a pulse. This switch SW4 in the ON state serves as the current path for applying a voltage to the scanning electrode Y side, in contrast with the common electrode X (at the ground).

[0084] Next, the switch SW5 is turned ON while the switch SW2 is kept ON. No power supply voltage is then supplied to the first signal line OUTA through the A/D converter 42 via the switch SW1, so the voltage of the first signal line OUTA remains at the ground level. Contrastingly as for the second signal line OUTB, the first signal line OUTA is grounded because the switch SW2 is ON. The second signal line OUTB has a potential (-Vs/2) lower than the ground level by a voltage (Vs/2) corresponding to the charges stored in the capacitor C1. Since the switch SW5 is ON, the voltage (-Vs/2) of the second signal line OUTB is applied to the load 20 through the output line OUTC. At this time, the switches SW3' and SW4' are turned ON to apply the voltage (-Vs/2) to the common electrode X side, in contrast with the scanning electrode Y (at Vs/2).

[0085] At the next timing, the switches SW2 and SW4 are set ON, and the remaining switches SW1, SW3, and SW5 are set OFF. The voltage of the output line OUTC is thereby raised to the ground level. After that, three switches SW1, SW3, and SW4 are set ON, and the remaining two switches SW2 and SW5 are set OFF, like the first stage. This operation is repeated after this.

[0086] Using the driving apparatus with this construction, the positive voltage (+Vs/2) and the negative voltage (-Vs/2) are alternately applied to the common electrode X of the load 20, as shown on the output line OUTC in Fig. 10. Also to the scanning electrode Y of the load 20, the positive voltage (+Vs/2) and the negative voltage (-Vs/2) are alternately applied by performing a switching control similar to that on the common electrode X side.

[0087] In this case, the respective voltages (±Vs/2) are applied to the common and scanning electrodes X and Y so that they are reverse in phase to each other. For example, when the positive voltage (+Vs/2) is applied to the common electrode X, the negative voltage (-Vs/2) is applied to the scanning electrode Y. By this manner, the potential difference between the common and scanning electrodes X and Y can be kept at the voltage Vs, which is equal to a sustain pulse. This makes it possible to provide the same state as that in the sustain discharge period shown in Fig. 3 (the state that the sustain pulse voltage Vs is applied alternately to the common and scanning electrodes X and Y).

[0088] Fig. 11 is a timing chart showing another example of driving waveforms in a sustain discharge period by the driving apparatus according to this embodiment.

[0089] Referring to Fig. 11, firstly, three switches SW1, SW3, and SW4 are turned ON, and the remaining switches SW2 and SW5 are kept OFF. At this time, the voltage of the first signal line OUTA rises to a voltage level (+Vs /2) given through the A/D converter 42 via the switch SW1, while the voltage of the second signal line OUTB remains at the ground level. Since the switch SW4 is ON, the voltage (+Vs/2) of the first signal line OUTA is applied to the load 20 via the output line OUTC.

[0090] At this stage, since the switches SW1 and SW3 are turned ON to connect the capacitor C1 to the power supply, charges corresponding to the voltage (Vs/2) given through the A/D converter 42 via the switch SW1 are stored in the capacitor C1.

[0091] At the next timing, all the five switches SW1 to SW5 are turned OFF. The first signal line OUTA is then at a high impedance to maintain its voltage (Vs/2), and the output line OUTC also maintains its voltage (Vs/2).

[0092] Next, two switches SW2 and SW5 are turned ON, and the remaining three switches SW1, SW3, and SW4 are kept OFF. No power supply voltage is then supplied to the first signal line OUTA through the A/D converter 42 via the switch SW1, so the voltage of the first signal line OUTA remains at the ground level.

[0093] As for the second signal line OUTB, the first signal line OUTA is grounded because the switch SW2 is ON. The second signal line OUTB has a potential (-Vs/2) lower than the ground level by a voltage (Vs/2) corresponding to the charges stored in the capacitor C1. Since the switch SW5 is ON, the voltage (-Vs/2) of the second signal line OUTB is applied to the load 20 through the output line OUTC.

[0094] At the next timing, all the five switches SW1 to SW5 are turned OFF again. The second signal line OUTB is then at a high impedance to maintain its voltage (-Vs/2), and the output line OUTC also maintains its voltage (-Vs/2). After that, three switches SW1, SW3, and SW4 are turned ON, and the remaining two switches SW2 and SW5 are kept OFF, like the first stage. This operation is repeated after this.

[0095] As described above, the driving apparatus shown in Fig. 9 according to the first embodiment of the present invention is characterized by including the first signal line OUTA the voltage on which changes between the Vs/2 level and the ground level in accordance with ON/OFF of the capacitor C1 and the switches SW1 to SW3, the second signal line OUTB the voltage on which changes between the ground level and the -Vs/2 level similarly, and the driver circuit for the load 20 provided between the first and second signal lines.

[0096] Using the driving apparatus with this construction, the positive voltage (+Vs/2) and the negative voltage (-Vs/2) are alternately applied to the common elec-

In addition, since it does not allow any countercurrent, no diode is required.

[0110] In the driving apparatus having the above construction, by the above switching control of the switches SW1 to SW5 on the common electrode X side and the switches SW1' to SW5' on the scanning electrode Y side, the positive and negative voltages (±Vs/2) are applied inversely in phase to the common and scanning electrodes X and Y.

[0111] In each sustain discharge period, the timing at which the voltage (+Vs/2 or -Vs/2) is applied to the common electrode X may not always be equal to the timing at which the voltage in the opposite phase (-Vs/2 or +Vs/2) is applied to the scanning electrode Y. The timings for both voltages may differ to some degree. For example, the voltage may be applied to one electrode after the voltage in the opposite phase applied to the other electrode has reached its stationary state. This causes a more stable action of sustain discharge.

[0112] The times of pulse voltages being applied to the electrodes X and Y need not always be equal to each other. The timings and times for applying voltages to the common and scanning electrodes X and Y can be controlled, e.g., by controlling ON/OFF timings of the switches SW4, SW4', SW5, and SW5'.

[0113] It is also possible to make, e.g., ON/OFF control of the above switches SW1 to SW5 and SW1' to SW5' in accordance with a program stored in a storage medium such as a ROM. This makes it possible to vary freely the waveform of voltage to be applied by changing ROM.

[0114] Figs. 14 to 20 show various examples of driving waveforms of pulse voltages to be applied to the electrodes X and Y in a sustain discharge period.

[0115] Fig. 14 shows an example of driving waveforms in which the timing of applying the positive voltage (+Vs/2) is always earlier than that of applying the negative voltage (-Vs/2), and the timing of returning the applied positive voltage (+Vs/2) to the ground level is always later than that of returning the applied negative voltage (-Vs/2) to the ground level. More specifically, after the positive voltage (+Vs/2) applied to one of the common or scanning electrodes X and Y has reached its stationary state, the negative voltage (-Vs/2) is applied to the other electrode. Besides, after the voltage being returned from the negative voltage (-Vs/2) to the ground level has reached its stationary state at one electrode, the voltage being applied to the other electrode is returned from the positive voltage (+Vs/2) to the ground level.

[0116] Furthermore, in this example of Fig. 14, the pulse width of the negative voltage (-Vs/2) is smaller than that of the positive voltage (+Vs/2) so that the negative voltage is returned to the ground level while the positive voltage is applied. This affords a more stable action of sustain discharge.

[0117] Fig. 15 shows an example of driving waveforms in which the relation in polarity is reversed to that in Fig. 14. That is, the timing of applying the negative voltage (-Vs/2) is always earlier than that of applying the positive voltage (+Vs/2), and the timing of returning the applied negative voltage (-Vs/2) to the ground level is always later than that of returning the applied positive voltage (+Vs/2) to the ground level. More specifically, after the negative voltage (-Vs/2) applied to one electrode has reached its stationary state, the positive voltage (+Vs/2) is applied to the other electrode. Besides, after the voltage being returned from the positive voltage (+Vs/2) to the ground level has reached its stationary state at one electrode, the voltage being applied to the other electrode is returned from the negative voltage (-Vs/2) to the ground level.

[0118] Furthermore, in this example of Fig. 15, the pulse width of the positive voltage (+Vs/2) is smaller than that of the negative voltage (-Vs/2) so that the positive voltage is returned to the ground level while the negative voltage is applied. This affords a more stable action of sustain discharge.

[0119] Fig. 16 shows an example of driving waveforms in which the negative voltage (-Vs/2) is used as the reference voltage. More specifically, in a sustain discharge period, both the electrodes X and Y are kept at the voltage (-Vs/2) while no sustain pulse is applied, and the voltage of one electrode is raised to (+Vs/2) at the timing of actually applying a sustain pulse to discharge. Also in this example of Fig. 16, the pulse width of the negative voltage (-Vs/2) is greater than that of the positive voltage (+Vs/2), like the example of Fig. 15.

[0120] As shown in this example of driving waveforms of Fig. 16, the voltage being applied to one electrode is fixed while the voltage being applied to the other electrode is changed. In this case, a predetermined voltage can be applied between the common and scanning electrodes X and Y only by such a change in voltage of the other electrode. This makes it possible to realize a more stable action of sustain discharge.

[0121] Fig. 17 shows an example of driving waveforms in which the relation in polarity is reversed to that in Fig. 16. That is, the positive voltage (+Vs/2) is used as the reference voltage. More specifically, in a sustain discharge period, both the electrodes X and Y are kept at the voltage (+Vs/2) while no sustain pulse is applied, and the voltage of one electrode is lowered to (-Vs/2) at the timing of actually applying a sustain pulse to cause a discharge. In this example of Fig. 17, the pulse width of the positive voltage (+Vs/2) is greater than that of the negative voltage (-Vs/2), like the example of Fig. 14.

[0122] As shown in this example of driving waveforms of Fig. 17, the voltage being applied to one electrode is fixed while the voltage being applied to the other electrode is changed. In this case, a predetermined voltage can be applied between the common and scanning electrodes X and Y only by such a change in voltage of the other electrode. This makes it possible to realize a more stable action of sustain discharge.

[0123] Fig. 18 shows an example of driving wave-

tween the electrodes X and Y of the load 20, and a sustain discharge occurs.

[0136] After applying the difference voltage (Vs) to the load 20 for the sustain discharge, on the common electrode X side, the switch SW4 is turned OFF to stop the supply of the voltage (+Vs/2). and then the switch SW5 is turned ON to return the voltage being applied to the common electrode X, to the ground level.

[0137] On the scanning electrode Y side, at a timing before the switch SW4 is turned OFF on the common electrode X side as described above, the switch SW5' is turned OFF to stop the supply of the voltage (-Vs/2), and then the switch SW4' is turned ON. In this manner, before the voltage being applied to the common electrode X is returned to the ground level, the voltage being applied to the scanning electrode Y is returned to the ground level.

[0138] At the next timing, all the five switches SW1 to SW5 on the common electrode X side and the five switches SW1' to SW5' on the scanning electrode Y side are OFF. Switch control completely reverse to the above on the common electrode X side and the scanning electrode Y side, is then performed so that the positive voltage (+Vs/2) with a large pulse width is applied to the scanning electrode Y side and the negative voltage (-Vs/2) with a pulse width smaller than that of the positive voltage on the scanning electrode Y side, is applied to the common electrode X side. After this, the same controls are repeated alternately.

[0139] Fig. 22 is a timing chart showing an example of control of the switches SW1 to SW5 and SW1' to SW5' to generate the waveforms on the electrodes X and Y shown in Fig. 15. In this example of Fig. 22, it is assumed that, by processing in the preceding subfield, the charges corresponding to the voltage (Vs/2) are stored in either of the capacitor C1 on the common electrode X side and the capacitor C4 on the scanning electrode Y side.

[0140] In sustain discharge period, on the scanning electrode Y side, firstly, two switches SW2' and SW5' are turned ON and the remaining switches SW1', SW3', and SW4' are kept OFF. Since the switch SW2' is turned ON and the first signal line OUTA' is grounded, the voltage of the fourth signal line OUTB' falls to the potential (-Vs/2), which is lower than the ground level by the voltage (Vs/2) corresponding to the charges stored in the capacitor C4. At this time, since the switch SW5' is turned ON simultaneously with the switch SW2', the voltage (-Vs/2) of the fourth signal line OUTB' is applied to the load 20 through the output line OUTC'.

[0141] On the common electrode X side, the switches SW1 and SW3 are turned ON at the same time when the switches SW2' and SW5' on the scanning electrode Y side are turned ON. After the negative voltage (-Vs/2) is applied to the scanning electrode Y side, the switch SW4 is also turned ON at a proper timing. In this state, the remaining two switches SW2 and SW5 are kept OFF.

[0142] The first signal line OUTA is thereby raised to the voltage level (+Vs/2) at the timing when the switch SW1 is turned ON. The voltage (+Vs/2) of this first signal line OUTA is output on the output line OUTC through the switch SW4, which has been turned ON at the proper timing, to be applied to the load 20. Thus the difference voltage (Vs) is applied between the electrodes X and Y of the load 20.

[0143] At this stage, the switches SW1 and SW3 are ON, and so the capacitor C1 is connected to the power supply. Thus the capacitor C1 stores the charges corresponding to the voltage (Vs/2) applied through the switch SW1.

[0144] After applying the difference voltage (Vs) to the load 20 for a sustain discharge, on the scanning electrode Y side, the switch SW5' is turned OFF to stop the supply of the voltage (-Vs/2), and then the switch SW4' is turned ON to return the voltage being applied to the scanning electrode Y, to the ground level.

[0145] On the common electrode X side, at a timing before the switch SW5' is turned OFF on the scanning electrode Y side as described above, the switch SW4 is turned OFF to stop the supply of the voltage (+Vs/2), and then the switch SW5 is turned ON. In this manner, before the voltage being applied to the scanning electrode Y is returned to the ground level, the voltage being applied to the common electrode X is returned to the ground level.

[0146] At the next timing, all the five switches SW1 to SW5 on the common electrode X side and the five switches SW1' to SW5' on the scanning electrode Y side are OFF. Switch control completely reverse to the above on the common electrode X side and the scanning electrode Y side, is then performed so that the negative voltage (-Vs/2) with a large pulse width is applied to the common electrode X side and the positive voltage (+Vs/2) with a pulse width smaller than that of the negative voltage on the common electrode X side, is applied to the scanning electrode Y side. After this, the same controls are repeated alternately.

[0147] Fig. 23 is a timing chart showing an example of control of the switches SW1 to SW5 and SW1' to SW5' to generate the waveforms on the electrodes X and Y shown in Fig. 16. In this example of Fig. 23, it is assumed that, by processing in the preceding subfield, the charges corresponding to the voltage (Vs/2) are stored in either of the capacitors C1 and C4 on the common electrode X side and the scanning electrode Y side.

[0148] In a sustain discharge period, on the common electrode X side, at first, the switches SW1, SW3, and SW4 are OFF and the remaining switches SW2 and SW5 are ON. This makes the state that the negative voltage (-Vs/2) is being applied to the common electrode X. Also on the scanning electrode Y side, at first, the switches SW1', SW3', and SW4' are OFF and the remaining switches SW2' and SW5' are ON, and this makes the state that the negative voltage (-Vs/2) is being applied to the scanning electrode Y.

[0149] At the next timing, on the common electrode X

controls are repeated alternately.

[0163] Fig. 25 is a timing chart showing an example of control of the switches SW1 to SW5 and SW1' to SW5' to generate the waveforms on the electrodes X and Y shown in Fig. 18. In this example of Fig. 25, it is assumed that, by processing in the preceding subfield, the charges corresponding to the voltage (Vs/2) are stored in either of the capacitors C1 and C4 on the common electrode X side and the scanning electrode Y side.

[0164] In a sustain discharge period, on the common electrode X side, at first, the switches SW1, SW3, and SW4 are OFF and the remaining switches SW2 and SW5 are ON. This makes the state that the negative voltage (-Vs/2) is being applied to the common electrode X. Also on the scanning electrode Y side, at first, the switches SW1', SW3', and SW4' are OFF and the remaining switches SW2' and SW5' are ON, and this makes the state that the negative voltage (-Vs/2) is being applied to the scanning electrode Y.

[0165] At the next timing, on the common electrode X side, after the switch SW5 is turned OFF to stop the supply of the voltage (-Vs/2), the switch SW4 is turned ON. The voltage being applied to the common electrode X is thereby returned to the ground level. Further, after the switch SW2 is turned OFF, the switches SW1 and SW3 are turned ON. At this time, the remaining switches SW4 and SW5 are kept ON and OFF, respectively.

[0166] In this manner, on the common electrode X side, the first signal line OUTA is raised to the voltage level (+Vs/2) applied through the switch SW1. The voltage (+Vs/2) of this first signal line OUTA is output on the output line OUTC through the switch SW4 to be applied to the load 20. At this time, the scanning electrode Y is kept in the state that the negative voltage (-Vs/2) is being applied thereto. Consequently, the difference voltage (Vs) is applied between the electrodes X and Y of the load 20, and a sustain discharge occurs.

[0167] At this stage, the switches SW1 and SW3 are ON, and so the capacitor C1 is connected to the power supply. Thus the capacitor C1 stores the charges corresponding to the voltage (Vs/2) applied through the switch SW1.

[0168] After applying the difference voltage (Vs) to the load 20 for the sustain discharge, on the scanning electrode Y side, the switch SW5' is turned OFF to stop the supply of the voltage (-Vs/2), and then the switch SW4' is turned ON to return the voltage being applied to the scanning electrode Y, to the ground level. Further, the switch SW2' is turned OFF, and then the switches SW1' and SW3' are turned ON. At this time, the remaining switches SW4' and SW5' are kept ON and OFF, respectively.

[0169] In this manner, on the scanning electrode Y side, the voltage of the third signal line OUTA' is raised to the voltage level (+Vs/2) applied through the switch SW1'. The voltage (+Vs/2) of this third signal line OUTA' is output on the output line OUTC' through the switch SW4' to be applied to the load 20. At this time, the common electrode X is kept in the state that the positive voltage (+Vs/2) is being applied thereto. Consequently, both electrodes X and Y of the load 20 are at the same potential.

[0170] Next, on the scanning electrode Y side, the switch SW4' is turned OFF to stop the supply of the voltage (+Vs/2), and then the switch SW5' is turned ON to return the voltage being applied to the scanning electrode Y, to the ground level. Further, the switches SW1' and SW3' are turned OFF, and then the switch SW2' is turned ON. At this time, the remaining switches SW4' and SW5' are kept OFF and ON, respectively.

[0171] Since the switch SW2' is turned ON and the first signal line OUTA' is grounded, the voltage of the fourth signal line OUTB' falls to the potential (-Vs/2), which is lower than the ground level by the voltage (Vs/2) corresponding to the charges stored in the capacitor C4. At this time, since the switch SW5' is ON, the voltage (-Vs/2) of the fourth signal line OUTB' is applied to the load 20 through the output line OUTC'.

[0172] On the common electrode X side, the switch SW4 is turned OFF synchronously with the switch SW4' on the scanning electrode Y side being turned OFF. The supply of the voltage (+Vs/2) is thereby stopped to make the common electrode X at a high impedance. Further, the switch SW5' is turned ON. The voltage of the common electrode X is thereby returned to the ground level by a function of the capacitance of the load 20, synchronously with the timing at which the voltage (+Vs/2) on the scanning electrode Y side is lowered to the ground level. After this, the switches SW1 and SW3 are turned OFF synchronously with the switches SW1' and SW3' on the scanning electrode Y side being turned OFF.

[0173] After this, the switch SW2 is turned ON synchronously with the switch SW2' on the scanning electrode Y side being turned ON in the state that the switch SW5' is kept ON. In this manner, by the function of the capacitance of the load 20, the voltage on the common electrode X side is lowered to the negative voltage (-Vs/2) with following the voltage on the scanning electrode Y side.

[0174] After the positive voltage (+Vs/2) is applied to the common electrode X, and the voltage being applied to the common electrode X is again returned to the negative voltage (-Vs/2), the same switching control is performed also on the scanning electrode Y side. By this control, also on the scanning electrode Y side, performed is the operation of applying the positive voltage (+Vs/2) and then returning to the state that the negative voltage (-Vs/2) is again applied. After this, the same controls are repeated alternately.

[0175] Fig. 26 is a timing chart showing another example of control of the switches SW1 to SW5 and SW1' to SW5' to generate the waveforms on the electrodes X and Y shown in Fig. 18. This example of Fig. 26 is almost the same as that of Fig. 25 described above, only except timings for turning the switches SW5 and SW5' ON.

[0176] More specifically, in the example of Fig. 25, the

[0189] The first signal line OUTA is thereby raised to the voltage level (+Vs/2) applied through the switch SW1. The voltage (+Vs/2) of this first signal line OUTA is output on the output line OUTC through the switch SW4, which has been turned ON at the proper timing, to be applied to the load 20. Thus the difference voltage (Vs) is applied between the electrodes X and Y of the load 20 to cause a sustain discharge.

[0190] At this stage, the switches SW1 and SW3 are ON, and so the capacitor C1 is connected to the power supply. Thus the capacitor C1 stores the charges corresponding to the voltage (Vs/2) applied through the switch SW1.

[0191] After applying the difference voltage (Vs) to the load 20 for the sustain discharge, on the scanning electrode Y side, the switch SW5' is turned OFF to stop the supply of the voltage (-Vs/2), and then the switch SW4' is turned ON to return the voltage being applied to the scanning electrode Y, to the ground level. Further, the switch SW2' is turned OFF, and then the switches SW1' and SW3' are turned ON. At this time, the remaining switches SW4' and SW5' are kept ON and OFF, respectively.

[0192] In this manner, on the scanning electrode Y side, the voltage of the third signal line OUTA' is raised to the voltage level (+Vs/2) applied through the switch SW1'. The voltage (+Vs/2) of this third signal line OUTA' is output on the output line OUTC' through the switch SW4' to be applied to the load 20. At this time, the common electrode X is kept in the state that the positive voltage (+Vs/2) is being applied thereto. Consequently, both electrodes X and Y of the load 20 are at the same potential.

[0193] Next, on the scanning electrode Y side, the switch SW4' is turned OFF to stop the supply of the voltage (+Vs/2). and then the switch SW5' is turned ON to return the voltage being applied to the scanning electrode Y, to the ground level.

[0194] On the common electrode X side, the switch SW4 is turned OFF synchronously with the switch SW4' on the scanning electrode Y side being turned OFF. At this time, since the switch SW5 is also OFF, the common electrode X becomes an high impedance state. In this manner, by the function of the capacitance of the load 20, the voltage on the common electrode X side is lowered to the ground level with following the voltage on the scanning electrode Y side.

[0195] After the negative and positive voltages (-Vs/2) and (+Vs/2) are respectively applied to the scanning and common electrodes Y and X to return the voltages of both electrodes X and Y to the ground level, switching control to the contrary is performed successively, thereby applying the positive and negative voltages (+Vs/2) and (-Vs/2) to the scanning and common electrodes Y and X sides, respectively. After this, the same controls are repeated alternately.

[0196] Fig. 29 is a timing chart showing another example of control of the switches SW1 to SW5 and SW1' to SW5' to generate the waveforms on the electrodes X and Y shown in Fig. 20. This example of Fig. 29 is almost the same as that of Fig. 28 described above, only except timings for turning the switches SW5 and SW5' ON.

[0197] More specifically, in the example of Fig. 28, after the difference voltage (Vs) is applied between the electrodes X and Y to make a sustain discharge occur, the switches SW4 and SW5 on the common electrode X side are set OFF to make a high impedance state on the common electrode X side. The voltage being applied to the common electrode X is lowered to (-Vs/2) with following the voltage drop on the scanning electrode Y side. Contrastingly in the example of Fig. 29, the switches SW4' and SW5' on the scanning electrode Y side are set OFF to make a high impedance state on the scanning electrode Y side, and the voltage being applied to the scanning electrode Y is lowered to (-Vs/2) with following the voltage drop on the common electrode X side.

[0198] Fig. 30 is a circuit diagram showing another example of construction of a driving apparatus according to this first embodiment. In Fig. 30, the components denoted by the same references as those in Fig. 9 or 12 have the same functions as those in Fig. 9 or 12, respectively. Thus the repetitive descriptions thereof will be omitted. Fig. 26 illustrates only the construction on the scanning electrode Y side in detail, but the power supply circuit 43 and the driver circuit 44 on the common electrode X side also have substantially the same constructions as the power supply circuit 43' and the driver circuit 44' on the scanning electrode Y side.

[0199] This example uses two capacitors C4 and C5 for storing charges on the scanning electrode Y side, and differs on this point from the example of Fig. 12 that uses only one capacitor C4. For example, an electrolytic capacitor and a film capacitor may be used as one capacitor C4 and the other capacitor C5, respectively. Use of such a film capacitor C5 in addition to an electrolytic capacitor C4 affords a stable operation even in a high frequency range. Besides, even in a low temperature condition in which the electrolytic capacitor C4 is hard to operate as a capacitance, the film capacitor C5 can compensate the operation. In case of the example of Fig. 5 using only one capacitor C4, the capacitor C4 may be either a film capacitor or an electrolytic capacitor.

[0200] Fig. 31 is a timing chart showing a specific example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 30. In Fig. 31, the parts shown by double lines in the driving waveforms of the third and fourth signal lines OUTA' and OUTB' and the output line OUTC', correspond to low impedance periods, i.e., periods in which any of the switches SW1' to SW5' is ON.

[0201] The features that, by switching operation of three switches SW1' to SW3', the voltage on the third signal line OUTA' is swung between the positive voltage (+Vs/2) and the ground level, and the voltage on the fourth signal line OUTB' is swung between the ground

clearly earlier than the timing of turning the switches SW1' and SW4' ON.

[0216] In case of controlling two or more switches to be changed at a time, those switches may not always simultaneously change due to various causes including unevenness in manufacturing elements, and there is a little time difference. In such a case, it is no problem if the timing of turning the switch SW3' ON is shifted to be earlier than the timing of turning the switches SW1' and SW4' ON. However, delay of the timing of turning the switch SW3' ON may cause a bad operation of the circuit. For this reason, in this example of Fig. 31, the timing of turning the switch SW3' ON is set to be clearly earlier, thereby insuring a stable operation of the circuit.

[0217] Besides in this example of Fig. 35, when two switches SW2' and SW5' are turned ON in order to output the negative voltage (-Vs/2) on the output line OUTC', the timing of turning the switch SW2' ON is set to be clearly earlier than the timing of turning the switch SW5' ON.

(Third Embodiment)

[0218] Next, the third embodiment of the present invention will be described.

[0219] Fig. 36 is a circuit diagram showing an example of construction of a driving apparatus according to this third embodiment. In Fig. 36, the components having the same functions as those in Fig. 9 are denoted by the same references as those in Fig. 9, respectively. Thus the repetitive descriptions thereof will be omitted.

[0220] In the driving apparatus shown in Fig. 9, the switch SW5 is provided in the driver circuit 44, and it and the switch SW4 are connected in series between both terminals of the capacitor C1 in the power supply circuit 43. Contrastingly in this third embodiment shown in Fig. 36, the switch SW5 is provided in the power supply circuit 43, and connected between the other terminal of the capacitor C1 and the second signal line OUTB. The other construction is the same as that in Fig. 9.

[0221] In this third embodiment shown in Fig. 36, for applying the positive voltage (+Vs/2) to the load 20 through the output line OUTC, the switches SW1 and SW4 are turned ON for example. Besides, for applying the negative voltage (-Vs/2) to the load 20 through the output line OUTC by using the charges stored in the capacitor C1, the switches SW2 and SW5 are turned ON. For this purpose, various patterns of driving waveforms like those described in the first embodiment can be used to be applied to the common and scanning electrodes X and Y.

[0222] According to this third embodiment thus constructed, the total voltage drop caused by a current flowing through switches at each timing when the capacitor of the load 20 is discharged, can be made small, and so the power loss is suppressed. More specifically, when the charges stored in the load 20 are eliminated to the ground line to return the load 20 from the positive voltage (+Vs/2) to the ground level, the current flows through two switches SW5 and SW3 in case of the first embodiment. Contrastingly in this third embodiment, the current flows through only one switch SW3 to discharge the load 20. Hence, the voltage drop can be decreased by the degree corresponding to one switch in comparison with the first embodiment.

[0223] Besides, in case of the driver circuit 44 constructed into an LSI as the eighth and ninth embodiments of the present invention which will be described later, it requires two switches SW4 and SW5 for every display line in case of the first embodiment. But the same according to this third embodiment only requires one switch SW5 for every display line, thereby considerably decreasing the total number of switches. This affords a reduced circuit scale and a cost reduction.

[0224] Fig. 37 is a circuit diagram showing another example of construction of a driving apparatus according to this third embodiment. In Fig. 37, the components having the same functions as those in Fig. 30 are denoted by the same references as those in Fig. 30, respectively. Thus the repetitive descriptions thereof will be omitted.

[0225] In this example of Fig. 37, the switch SW5' is provided in the power supply circuit 43', and connected between the other terminal of each of the capacitors C4 and C5, and the fourth signal lines OUTB'. The other construction is the same as that in Fig. 30.

[0226] Fig. 38 is a timing chart showing a specific example of driving waveforms in a sustain discharge period by the driving apparatus constructed as in Fig. 37.

[0227] The basic operations for alternately applying the positive and negative voltages (±Vs/2) on the output line OUTC' by switching control of the five switches SW1' to SW5' are the same as those in the first embodiment described above. Thus the detailed description thereof will be omitted here.

[0228] It should be noted in Fig. 38 that the switches SW3' and SW5' are not turned ON when the switches SW1' and SW4' are turned ON to apply the positive voltage (+Vs/2) to the load 20, but those switches SW3' and SW5' are turned ON when the charges stored in the load 20 by the application of the positive voltage (+Vs/2) are eliminated to return the voltage being applied, to the ground level. In this example of Fig. 38, by keeping the switch SW1' ON till the switch SW3' is turned ON, the capacitors C4 and C5 are charged at the timing of discharging the load 20. In this manner, changeover of each of the switches SW1' to SW5' can be made more effectively without useless.

[0229] Besides, in this example of Fig. 38, the timing of turning the switch SW1' ON is clearly earlier than the timing of turning the switch SW4' ON. This is for insuring a stable operation of the circuit like the second embodiment described with Fig. 35, by the manner that not the changeover timings of the switches SW1' and SW4' are set at the same timing but the timing of turning the switch SW1' ON is set to be clearly earlier.

of pulse voltage being applied to the scanning electrode Y, obtuse by the function of a resistor R2 connected to the transistor Tr21. This transistor Tr21 and the resistor R2 are connected in parallel with the switch SW5'.

[0248] The transistors Tr22 and Tr23 are for giving the potential difference (Vs/2) between both terminals of the scan driver 31' in address period. This is by the following reason. In sustain discharge period, the switches SW2' and SW5' are turned ON. The upper side voltage of the scan driver 31' thereby becomes (-Vs/2) in accordance with the charges accumulated in the capacitor C4, but the lower side voltage of the scan driver 31' also becomes (-Vs/2) by a function of the diode in the scan driver 31'. Thus the potential difference (Vs/2) can not be given between both terminals of the scan driver 31'.

[0249] Contrastingly in address period, the switch SW2' and the transistor Tr22 are turned ON. The upper side voltage of the scan driver 31' thereby becomes the ground level. Besides, the transistor Tr23 is turned ON at this time. The negative voltage (-Vs/2) output on the fourth signal line OUTB' in accordance with the charges accumulated in the capacitor C4 is thereby applied to the lower side of the scan driver 31'. In outputting a scan pulse by the scan driver 31', the negative voltage (-Vs/2) can be applied to the scanning electrode Y.

[0250] One diode D16 is used when a current is made to flow from the scan driver 31' to the ground at the timing of applying the positive voltage (+Vs/2) to the common electrode X. For the current flowing from the scan driver 31' to the ground, a route in case of turning the switch SW2' ON and a route in case of turning the switches SW3' and SW5' ON are present. In this example, however, the diode D16 is provided in the middle of the route on the switch SW2' side so that the current may be made to flow through the switch SW2' to the ground. In this manner, the total voltage drop caused by the current flowing through switches, can be made small, and so the power loss is suppressed.

[0251] The other diode D17 is used when a current is made to flow from the ground to the scan driver 31' at the timing of returning the voltage being applied to the common electrode X, from the positive voltage (+Vs/2) to the ground level. For the current flowing from the ground to the scan driver 31', thinkable are the route through the switch SW3', the fourth signal line OUTB', and the diode D17, and the route through the switch SW2', the third signal line OUTA', and the switch SW4'. In this example, however, the diode D17 is provided so that the current may be made to flow through this route. The number of stages of switches to pass through is thereby reduced, and the total voltage drop can be made small.

[0252] Fig. 43 is a timing chart showing driving waveforms on the scanning electrode Y side by the driving apparatus constructed as in Fig. 42, which shows only the reset and sustain discharge periods in one subfield.

[0253] Referring to Fig. 43, in reset period, the switches SW1' and SW3' are turned ON to accumulate the charges corresponding to the voltage (Vs/2) in the capacitor C4. After this, the switches SW1' and SW3' are turned OFF, and then the switch SW9' as well as the switch SW4' is turned ON. The voltage of the third signal line OUTA' is thereby raised to the voltage level corresponding to the sum of the voltage (Vs/2) of the capacitor C4 and the voltage Vw of the fourth signal line OUTB'. The voltage (Vs/2 + Vw) is applied to the scanning electrode Y of the load 20. At this time, as shown in Fig. 43, the voltage rises gradually by the function of the resistor R1 provided in the switch SW9'.

[0254] At this time, by applying the negative voltage (-Vs/2) to the common electrode X, the potential difference between the common and scanning electrodes X and Y becomes (Vs + Vw). The same potential difference as the full write pulse shown in the reset period of Fig. 3 can be thereby applied between the common and scanning electrodes X and Y. In this case, the voltage applied to the element of the switch SW9' is Vw at most. Thus the breakdown voltage of this element may be set at Vw, and it can be held down to a considerably low value in comparison with its breakdown voltage in previously-considered apparatus.

[0255] Besides, since the voltages between the third and fourth signal lines OUTA' and OUTB' and between the first and second signal lines OUTA and OUTB are always Vs/2 or less, the breakdown voltage of each of the switches SW4', SW5', SW4, and SW5, and the scan driver 31' may be Vs/2 or more. This makes it possible to apply the full write pulse voltage (Vs + Vw) between the common and scanning electrodes X and Y using a circuit with a low breakdown voltage, and so realize a reduced cost in manufacturing.

[0256] In the sustain discharge period, the switch SW9' is not turned ON, and the other switches SW1' to SW5' are controlled in the same manner as in the above embodiments so that the positive and negative voltages (±Vs/2) are alternately applied to the scanning electrode Y of the load 20.

[0257] Fig. 44 is a circuit diagram showing another example of construction of a driving apparatus according to this fifth embodiment. In Fig. 44, the components having the same functions as those in Fig. 42 are denoted by the same references as those in Fig. 42, respectively. Thus the repetitive descriptions thereof will be omitted.

[0258] In this example of Fig. 44, a circuit for applying a voltage Vw' is provided on the scanning electrode Y side. More specifically, the switch SW9' is provided between the power supply line for the voltage Vw' and the fourth signal line OUTB'. This switch SW9' includes a resistor R1. This power supply voltage Vw' is greater than the voltage (Vs/2). For example, it has the same voltage value as the full write pulse voltage (Vs/2 + Vw) applied to the load 20 in the reset period.

[0259] In this construction, to apply the voltage Vw' to the load 20, the switch SW9' is turned ON. The voltage Vw' is thereby applied through the route of the diode D17 provided in parallel with the transistor Tr 23, and a diode

20 when the scanning electrode Y is selected in a line-sequential manner. When the scanning electrode Y is not selected, the voltage at the ground level is applied to it.

[0272] At this time, an address pulse of the voltage Va is selectively applied to an address electrode Aj corresponding to the cell in which a sustain discharge should occur, i.e., the cell to be lit, in the address electrodes A1 to Am. As a result, a discharge occurs between the address electrode Aj and the scanning electrode Y selected in the line-sequential manner, of the cell to be lit, and it serves as a priming (pilot) for a discharge immediately occurring between the common and scanning electrodes X and Y. A quantity of wall charges for making the next sustain discharge possible is thereby stored in the surface of the MgO protective film on the common and scanning electrodes X and Y of the selected cell.

[0273] The discharge between the address and scanning electrodes Aj and Y is started by the potential difference (Va + Vs/2) between the electrodes. Thus the discharge can be started at a lower voltage than the conventional potential difference (Va + Vy). This is adjusted by applying an obtuse wave in the reset period as described above, causing a weak discharge to occur, and thereby not completely eliminating the wall charges on the scanning electrode Y to leave some wall charges there. In short, when the sum of the voltage corresponding to the remaining wall charges and the voltage being applied reaches the discharge start voltage, the discharge starts.

[0274] For this reason, the driving apparatus according to this embodiment requires no power supply for generating the voltage -Vy in the address period, unlike the prior art. Thus it does not require also the switching circuit such as the transistor Tr14 for disconnecting the power supply line of the voltage -Vy as shown in Fig. 4. Furthermore, as clearly when Figs. 45 and 3 are compared, the driving apparatus according to this embodiment also requires no power supply for generating the non-selection pulse voltage -Vsc in the address period. This makes it possible to simplify the circuit construction accordingly.

[0275] After this, in the sustain discharge period, the voltages (+Vs/2 and -Vs/2) in opposite phases to each other are alternately applied to the common electrode X and the scanning electrode Y of each display line to make sustain discharges occur, and an image display of one subfield is made.

[0276] During this sustain discharge period, the potentials of the address electrodes A1 to Am are kept at the ground level. In general, the address electrodes A1 to Am are preferably set at the middle potential between the voltages to be applied respectively to the common and scanning electrodes X and Y during the sustain discharge period. For this reason, in the conventional driving apparatus as shown in Fig. 3, the address electrodes A1 to Am must be set at (Vs/2) that is the middle potential between the common and scanning electrodes X and Y. Contrastingly in this embodiment, the middle potential between the common and scanning electrodes X and Y is the ground level. Thus it is not required to raise the potentials of the address electrodes A1 to Am to (Vs/2), and any circuit for that purpose may not be provided.

[0277] Fig. 46 is a circuit diagram showing another example of construction of a driving apparatus according to this fifth embodiment. In Fig. 46, the components having the same functions as those in Fig. 44 are denoted by the same references as those in Fig. 44, respectively. Thus the repetitive descriptions thereof will be omitted.

[0278] In the above example of Fig. 44, the circuit for applying the voltage Vw' is provided on the scanning electrode Y side. Contrastingly in the example of Fig. 46, on the common electrode X side, a switch SW10 with a resistor R3 is provided between the first signal line OUTA and the output line OUTC, and a switch SW11 with a resistor R4 and a power supply for a voltage Vwn are provided between the first signal line OUTA and the ground.

[0279] By turning the switch SW10 ON, the positive voltage (+Vs/2) is gradually applied to the common electrode X of the load 20 by the function of the resistor R3. By turning the switch SW11 ON, the negative voltage (-Vwn) is gradually applied to the common electrode X of the load 20 by the function of the resistor R4.

[0280] Fig. 47 is a timing chart showing driving waveforms on the common electrode X side by the driving apparatus constructed as in Fig. 46, which shows only the reset and sustain discharge periods in one subfield.

[0281] Referring to Fig. 47, in reset period, firstly by turning the switch SW11 ON, the negative voltage (-Vwn) is gradually applied to the common electrode X of the load 20. At this time, the switches SW2 and SW5 may be also turned ON so as to add the voltage (-Vs/2) by utilizing the charges stored in the capacitor C1, thereby applying the voltage -(Vwn + Vs/2). Next, the switches SW11 and SW5 are turned OFF, and the switches SW2 and SW4 are turned ON, so that the voltage of the common electrode X becomes the ground level. Next, by setting the switches SW2, SW4, SW5, and SW11 OFF, and the remaining switches SW1, SW3, and SW10 ON, the positive voltage (+Vs/2) is gradually applied to the common electrode X of the load 20.

[0282] In the subsequent sustain discharge period, the switches SW10 and SW11 are not turned ON, and the other switches SW1 to SW5 are controlled like the above embodiments so as alternately to apply the positive and negative voltages (±Vs/2) to the common electrode X.

(Sixth Embodiment)

[0283] Next, the sixth embodiment of the present invention will be described.

[0284] In this sixth embodiment, a power recovery circuit is further provided for the circuit shown in each of the above first to fifth embodiments.

[0285] Fig. 48 is a circuit diagram showing a specific

with the charges accumulated in the capacitor C4 is applied to the output line OUTC'. The voltage (Vs/2 + Vw) is applied to the scanning electrode Y of the load 20. At this time, the voltage gradually rises by the function of the resistor R1' in the switch SW9'.

[0298] Since the potential difference between the common and scanning electrodes X and Y thereby becomes (Vs + Vw), the same voltage as that of the full write pulse shown in the reset period in Fig. 3 can be applied between the common and scanning electrodes X and Y.

[0299] Next, all the switches SW1 to SW5, SW9, SW1' to SW5', and SW9' are properly controlled to return the voltages being applied to the common and scanning electrodes X and Y, to the ground level. The common electrode X side and the scanning electrode Y side are then made in the states reverse to those described above. More specifically, on the common electrode X side, the switches SW1, SW4, and SW9 are turned ON, and the remaining switches SW2, SW3, and SW5 are turned OFF. At the same time, on the scanning electrode Y side, the switches SW2' and SW5' are turned ON, and the remaining switches SW1', SW3', SW4', and SW9' are turned OFF.

[0300] The voltage being applied to the common electrode X thereby continuously rises from the ground level to (Vs/2 + Vw), and the voltage being applied to the scanning electrode Y is lowered to (-Vs/2). In every cell, the voltage due to the wall charges themselves then exceeds its discharge start voltage, and a discharge starts. At this time, weak discharges occur by applying the obtuse wave so that the accumulated wall charges are eliminated except part of them.

[0301] In this reset period, by turning the transistor Tr21 ON, the voltage being applied to the scanning electrode Y may be continuously lowered from the ground level to the (-Vs/2) level, as indicated by a dotted line. Also the voltage being applied to the common electrode X can be continuously lowered from the ground level to the (-Vs/2) level, as indicated by another dotted line, if the same components as the above transistor Tr21 and resistor R2 are provided in parallel with the switch SW5 on the common electrode X side.

[0302] Fig. 50 is a timing chart showing a manner of power recovery in each of the power recovery circuits 22 and 33 showing in Fig. 48. On the common electrode X side, the switches SW1 and SW3 are turned ON to apply the positive voltage (+Vs/2) is applied on the first signal line OUTA. When the voltage of the second signal line OUTB is at the ground level, the transistor Tr3 in the power recovery circuit 22 is turned ON. An L-C resonance thereby occur with the coil L1 and the capacitance of the load 20 due to the potential difference between the above capacitor C2 and the common electrode X at the ground level. The charges having been recovered in the capacitor C2 are then supplied to the load 20 via the transistor Tr3, the diode D3, and the coil L1.

[0303] At this time, on the scanning electrode Y side, since the switch SW2' is ON, the current supplied from the capacitor C2 through the switch SW3 on the common electrode X side to the common electrode X flows through the diode in the scan driver 31' and the diode D16 on the scanning electrode Y side, and then flows into the ground through the third signal line OUTA' and the switch SW2'. With such a current flow, the voltage of the common electrode X gradually rises as shown in Fig. 50. By turning the switch SW4 ON near a peak voltage appearing in this resonance, the voltage of the common electrode X is clamped to (Vs/2).

[0304] Next, further on the scanning electrode Y side, the transistor Tr15 in the power recovery circuit 33 is turned ON. An L-C resonance thereby occur with the coil L3 and the capacitance of the load 20 due to the potential difference between the voltage of the capacitor C3 and the voltage of the scanning electrode Y at the ground level. The current supplied from the capacitor C1 through the switch SW3 on the common electrode X side to the common electrode X via the first signal line OUTA and switch SW4, flows through the diode in the scan driver 31' and the diode D12 in the power recovery circuit 33 on the scanning electrode Y side, and further flows through the transistor Tr15, the capacitors C3 and C4, and the switch SW2' into the ground. With such a current flow, the voltage of the scanning electrode Y is gradually lowered as shown in Fig. 50. At this time, part of the charges can be recovered in the capacitor C3. By further turning the switch SW5' ON near a peak voltage appearing in this resonance, the voltage of the scanning electrode Y is clamped to (-Vs/2).

[0305] Next, in this state, on the scanning electrode Y side, the switch SW2' and the transistor Tr16 in the power recovery circuit 33 are set ON. An L-C resonance thereby occur with the coil L4 and the capacitance of the load 20 due to the potential difference between the voltage of the capacitor C3 and the voltage (-Vs/2) of the scanning electrode Y. The charges recovered in the capacitor C3 are then supplied to the load 20 through the transistor Tr16, the diode D13, the coil L4, and the diode in the scan driver 31'.

[0306] At this time, on the common electrode X side, since the switches SW1, SW3, and SW4 are ON, the current supplied from the capacitor C3 through the switch SW2' and the capacitor C4 on the scanning electrode Y side to the scanning electrode Y flows through the switch SW4 on the common electrode X side, and then flows into the ground through the first signal line OUTA, the capacitor C1, and the switch SW3. With such a current flow, the voltage of the scanning electrode Y gradually rises as shown in Fig. 50. By further turning the switch SW4' ON near a peak voltage appearing in this resonance, the voltage of the scanning electrode Y is clamped to the ground level.

[0307] Next, on the common electrode X side, the switches SW1 and SW3 and the transistor Tr4 in the power recovery circuit 22 are set ON. An L-C resonance

apparatus shown in Fig. 51 is provided with a power recovery circuit 22 comprising two systems of coils L1 and L2, like the driving apparatus shown in Fig. 48. The coils L1 and L2 are isolated from the common electrode X of the load 20 (output line OUTC) by diodes D7and D8. The diodes D18 and D19 respectively connected between the coil L1 of the power recovery circuit 22 and the second signal line OUTB, and between the coil L2 and the first signal line OUTA, have the same roles as the diodes D16 and D17 on the scanning electrode Y side.

[0317] The power recovery circuit 22 further comprises four diodes D20 to D23 for clamping. The diodes 20 and 21 are connected in series between the first and second signal lines OUTA and OUTB. The node between the diodes is connected between the cathode of the diode D3 and the coil L1. The diodes 22 and 23 are also connected in series between the first and second signal lines OUTA and OUTB. The node between the diodes is connected between the anode of the diode D4 and the coil L2.

[0318] The power recovery circuit 22 shown in Fig. 51 further comprises two capacitors C2 and C12 for power recovery. The capacitor C12, which is newly provided in this example of Fig. 51, is connected between a common terminal of two transistors Tr3 and Tr4, and the first signal line OUTA.

[0319] By the provision of this capacitor C12, when the voltage of the first signal line OUTA is to be set at the ground level by turning the switch SW2 ON, the power of the first signal line OUTA can be recovered or supplied as it is, in relation to the capacitance of the load 20, using the capacitor C12 without passing through the capacitors C1 and C2, thereby decreasing power loss.

[0320] More specifically, when the power recovery circuit 22 comprises only the capacitor C2 as shown in Fig. 48, power recovery is performed by the manner that a current flows in the route of the capacitors C2 and C1 and the switch SW2. That is, the current flows through two capacitors. Contrastingly in case of also providing the capacitor C12 as shown in Fig. 51, power recovery is performed by the manner that a current flows in the route of the capacitor C12 and the switch SW2. That is, the current flows through only one capacitor. Consequently, in case of Fig. 51, power loss due to the impedance components caused by capacitors is a little, so the power recovery efficiency can be improved.

[0321] Fig. 52 is a timing chart showing the manner of power recovery by the power recovery circuit 22 shown in Fig. 51. When the switches SW1 and SW3 are ON to apply the positive voltage (+Vs/2) to the first signal line OUTA, and the second signal line OUTB is at the ground level, the voltage of the node between the capacitors C2 and C12 is Vs/4.

[0322] In this state, when the transistor Tr3 in the power recovery circuit 22 is turned ON, an L-C resonance occurs with the coil L1 and the capacitance of the load 20 due to the potential difference (Vs/4) between the above node between the capacitors C2 and C12, and the common electrode X, which is at the ground level. The voltage of the common electrode X thereby gradually rises as shown in Fig. 52, using the power having been recovered in the capacitors C2 and C12. By turning the switch SW4 ON near a peak voltage appearing in this resonance, the voltage of the common electrode X is clamped to (Vs/2).

[0323] Further, in this state, when the transistor Tr3 and the switch SW4 are turned OFF, and the transistor Tr4 in the power recovery circuit 22 is turned ON, an L-C resonance occurs with the coil L2 and the capacitance of the load 20 due to the potential difference (Vs/4) between the voltage (Vs/4) of the above node between the capacitors C2 and C12, and the voltage (Vs/2) of the common electrode X. The voltage of the common electrode X is thereby gradually lowered as shown in Fig. 52. At this time, part of the charges can be recovered in the capacitors C2 and C12. By turning the switch SW5 ON near a peak voltage appearing in this resonance, the voltage of the common electrode X is clamped to the ground level.

[0324] Next, the switch SW2 is turned ON to set the voltages of the first and second signal lines OUTA and OUTB at the ground level and the negative voltage (-Vs/2), respectively. The voltage of the node between the capacitors C2 and C12 then becomes (-Vs/4).

[0325] In this state, when the transistor Tr4 in the power recovery circuit 22 is turned ON, an L-C resonance occurs with the coil L2 and the capacitance of the load 20 due to the potential difference (Vs/4) between the above node between the capacitors C2 and C12, and the common electrode X, which is at the ground level. The voltage of the common electrode X is thereby gradually lowered as shown in Fig. 52. At this time, part of the charges can be recovered in the capacitors C2 and C12. By turning the switch SW5 ON near a peak voltage appearing in this resonance, the voltage of the common electrode X is clamped to (-Vs/2).

[0326] Further, in this state, when the transistor TR4, and the switch SW5 are turned OFF, and the transistor Tr3 in the power recovery circuit 22 is turned ON, an L-C resonance occurs with the coil L1 and the capacitance of the load 20 due to the potential difference (Vs/4) between the voltage (-Vs/4) of the above node between the capacitors C2 and C12, and the voltage (-Vs/2) of the common electrode X. The voltage of the common electrode X thereby gradually rises as shown in Fig. 52, using the power having been recovered in the capacitors C2 and C12. By turning the switch SW4 ON near a peak voltage appearing in this resonance, the voltage of the common electrode X is clamped to the ground level.

[0327] In this manner, according to the example of construction of Fig. 51, by the provision of the two capacitors C2 and C12 between the first and second signal lines OUTA and OUTB for power recovery, two stages of power recovery can be performed with a small circuit

Fig. 54, on the common electrode X side, there are not provided the diodes D7, D8, D18, and D19 which are provided in the example of Fig. 51. Thus the coils L1 and L2 can be directly seen from the common electrode X side. Besides, in either of the common electrode X side and the scanning electrode Y side, the capacitors C12 and C13 may be provided which are provided in the example of Fig. 51.

[0341] Fig. 55 is a circuit diagram showing another example of construction of a driving apparatus according to this sixth embodiment. In Fig. 55, the components having the same functions as those in Fig. 51 are denoted by the same references as those in Fig. 51, respectively. Thus the repetitive descriptions thereof will be omitted.

[0342] The construction shown in Fig. 55 differs from the construction shown in Fig. 51 only in the point of absence of the capacitors C12 and C13, in the feature of connection in relation to the diodes D20 to D23 and D20' to D23' for clamping, and in the feature that the coils L1 and L2 are not isolated from the common electrode X of the load 20 (output line OUTC) by using the diodes D7 and D8.

[0343] More specifically, in the construction shown in Fig. 55, in the power recovery circuit 22 on the common electrode X side, the node between the diodes D20 and D21, which are connected in series between the first and second signal lines OUTA and OUTB, is connected between the cathode of the diode D4 and the transistor Tr4. Besides, the node between the diodes D22 and D23, which are also connected in series between the first and second signal lines OUTA and OUTB, is connected between the anode of the diode D3 and the transistor Tr3.

[0344] In the power recovery circuit 33 on the scanning electrode Y side, the node between the diodes D20' and D21', which are connected in series between the third and fourth signal lines OUTA' and OUTB', is connected between the anode of the diode D13 and the transistor Tr16. Besides, the node between the diodes D22' and D23', which are also connected in series between the third and fourth signal lines OUTA' and OUTB', is connected between the cathode of the diode D12 and the transistor Tr15.

[0345] On the common electrode X side, there are not provided the diodes D7, D8, D18, and D19 which are provided in the example of Fig. 51. Thus the coils L1 and L2 can be directly seen from the common electrode X side. Besides, in either of the common electrode X side and the scanning electrode Y side, the capacitors C12 and C13 may be provided which are provided in the example of Fig. 51.

[0346] Fig. 56 is a circuit diagram showing another example of construction of a driving apparatus according to this sixth embodiment. In Fig. 56, the components having the same functions as those in Fig. 51 are denoted by the same references as those in Fig. 51, respectively. Thus the repetitive descriptions thereof will be omitted.

[0347] The construction shown in Fig. 56 differs from the construction shown in Fig. 51 only in the point of absence of the capacitors C12 and C13, in the feature that the power recovery circuit 22 on the common electrode X side is made up from only one system of the coil L1, and in the feature that the coil L1 is not isolated from the common electrode X of the load 20 (output line OUTC) by using the diodes D7 and D8.

[0348] More specifically, in the construction shown in Fig. 56, in the power recovery circuit 22 on the common electrode X side, the node between the diodes D20 and D21, which are connected in series between the first and second signal lines OUTA and OUTB, is connected between the cathode of the diode D3 and the coil L1. The coil L2 and the diodes D22 and D23 which are provided in the example of Fig. 51, are not provided in this construction shown in Fig. 56.

[0349] On the common electrode X side, there are not provided the diodes D7, D8, D18, and D19 which are provided in the example of Fig. 51. Thus the coil L1 can be directly seen from the common electrode X side. Besides, in either of the common electrode X side and the scanning electrode Y side, the capacitors C12 and C13 may be provided which are provided in the example of Fig. 51.

[0350] Since the power recovery circuit 22 is made up from only one system of the coil L1, a simple circuit construction can be obtained.

[0351] Fig. 57 is a circuit diagram showing another example of construction of a driving apparatus according to this sixth embodiment. In Fig. 57, the components having the same functions as those in Fig. 56 are denoted by the same references as those in Fig. 56, respectively. Thus the repetitive descriptions thereof will be omitted.

[0352] The construction shown in Fig. 57 differs from the construction shown in Fig. 56 only in the feature of using four diodes D20 to D23 for clamping in the power recovery circuit 22 on the common electrode X side, in the feature of connection in relation to them, and in the feature of connection in relation to the diodes D20' to D23' on the scanning electrode Y side.

[0353] More specifically, in the construction shown in Fig. 57, in the power recovery circuit 22 on the common electrode X side, the node between the diodes D20 and D21, which are connected in series between the first and second signal lines OUTA and OUTB, is connected between the cathode of the diode D4 and the transistor Tr4. Besides, the node between the diodes D22 and D23, which are also connected in series between the first and second signal lines OUTA and OUTB, is connected between the anode of the diode D3 and the transistor Tr3. The construction on the scanning electrode Y side is quite the same as that in Fig. 53.

[0354] Fig. 58 is a circuit diagram showing another example of construction of a driving apparatus according to this sixth embodiment. In Fig. 58, the components

trode X and Y in the scan pulse becomes (Vx + Vs/2) + Vs/2 = 230 V.

[0369] At this time, since the voltage difference (Vs/2) between the first and second signal lines OUTA and OUTB is applied to the FETs (switches SW4 and SW5) for treating the above discharge current, the breakdown voltage of each of the FETs is sufficed by Vs/2 or more. This shows that the potential difference 230 V between the electrodes X and Y in the scan pulse shown in Fig. 7 can be realized by the low-voltage circuit according to this embodiment.

[0370] Since the voltage Va of the address electrode A is 60 V and the scan pulse voltage of the scanning electrode Y is (-Vs/2 = -90 V), the potential difference between the address and scanning electrodes A and Y in the address period is 150 V. This potential difference is less than the potential difference 240 V between the address and scanning electrodes A and Y shown in Fig. 7. In this relation, in the subsequent reset period, wall charges can easily be accumulated in the dielectric layer on the address electrode A. In the reset period, the wall charges of 240 V - 150 V = 90 V are accumulated. By the above manner, the same operation as that in Fig. 7 is performed.

[0371] The operation in sustain discharge period is the same as that shown in Fig. 49, and the potential difference between the first and second signal lines OUTA and OUTB is always Vs/2. Since the switches SW4 and SW5, or SW4' and SW5' for exchanging the gas discharge current shown in Fig. 60 are disposed within the first and second signal lines OUTA and OUTB, or the third and fourth signal lines OUTA' and OUTB', the breakdown voltage of the FET making up each of the switches is sufficed by Vs/2 or more.

[0372] In this manner, since the breakdown voltage of each FET is held down to half the conventional value, the ON resistance of the FET can be considerably reduced. Consequently, the number of elements can be considerably reduced though the prior art requires a number of FETs provided in parallel for realizing a stable gas discharge. Besides, the unit cost of element itself can be reduced because of its low breakdown voltage. Further, the high-voltage power supply required for driving is sufficed by two kinds of Vs/2 (90 V) and Vx (50 V). This makes it possible to omit some power supplies. It should be noted that the cost of the additional circuit according to this embodiment is substantially the same as that of the A/S separation circuit used in the prior art shown in Fig. 5. Therefore, with the above-described construction, an inexpensive PDP can be realized.

[0373] The above-described embodiment is provided with a power recovery circuit. Since the power in case of no power recovery circuit is proportional to $Cp \cdot V^2 \cdot f$, the power loss can be held down to half the conventional one. Therefore, such a power recovery circuit can be omitted. Fig. 62 shows a circuit with no power recovery circuit. The output waveforms in sustain discharge period are the same as those shown in Fig. 21. The output waveforms in line-sequential scanning period are the same as those shown in Fig. 61.

[0374] When the power recovery circuit is provided, a circuit (the switches SW4' and SW5' shown in Fig. 60) is required for clamping to the power supply after outputting the L-C resonance voltage, as shown in Fig. 60. But, since the power recovery circuit can be omitted, charging and discharging currents and a gas discharge current can be made to flow to the load capacitance Cp through the FETs of the scan driver comprising only the switches SW4' and SW5' shown in Fig. 62. In sustain discharge period, the switch SW4' is turned ON when the voltage of the third signal line OUTA' is applied to the scanning electrode Y, and the switch SW5' is turned ON when the voltage of the fourth signal line OUTB' is applied to the scanning electrode Y

[0375] As for the operation on the scanning electrode Y side in line-sequential scanning period, by turning the switch SW2' ON, the voltages of the third and fourth signal lines OUTA' and OUTB' are set at the ground level and (-Vs/2), respectively. The voltages of both terminals of the scan driver are thereby set at the ground level and (-Vs/2), respectively. In scanning, the scan pulse voltage (-Vs/2) is output to the scanning electrode Y.

[0376] As described above, by omitting the power recovery circuit, in addition to the above-described effects according to the construction shown in Fig. 60, the number of circuits can be reduced more. This makes it possible to realize a PDP at a more reduced cost.

(Seventh Embodiment)

[0377] Next, the seventh embodiment of the present invention will be described.

[0378] In this seventh embodiment, a circuit for applying a voltage for the address period, the reset period, or scan from each independent power supply through switching elements, is further provided for the circuit shown in each of the above first to sixth embodiments.

[0379] Fig. 63 is a circuit diagram showing a specific example of construction of a driving apparatus according to this seventh embodiment. Fig. 63 shows a construction for driving associated with not only a sustain discharge period but also reset and address periods. In Fig. 63, the components having the same functions as those in Fig. 12 or 42, etc., are denoted by the same references as those in Fig. 12 or 42, etc., respectively. Thus the repetitive descriptions thereof will be omitted.

[0380] Referring to Fig. 63, on the common electrode X side, a switch SW8 is provided between the power supply line for generating a voltage Vx, and the second signal line OUTB. On the scanning electrode Y side, a switch SW9' is provided between the power supply line for generating the voltage Vw, and the fourth signal line OUTB'.

[0381] Fig. 64 is a timing chart showing driving waveforms of the PDP by the driving apparatus constructed as shown in Fig. 63. Fig. 64 shows one of the subfields

as a scan driver circuit. That is, such a driver circuit 51' is provided for every display line of the PDP. Namely, there are provided the same numbers of switches SW4' and SW5' as the number of display lines.

[0396] Contrastingly, the driver circuit 44 on the common electrode X side is provided in common for all display lines of the PDP, like the power supply circuit 43.

[0397] In this construction, at least on the scanning electrode Y side, by switching control of the switches SW4' and SW5' provided for each display line, in the sustain discharge period, the voltage to be applied to the display line can be controlled individually. Besides, the transistors Tr22 and Tr23 in the above-described embodiments, which are the switching elements for applying the voltage (-Vs/2) in the address period, can be omitted.

[0398] Fig. 68 is a circuit diagram showing another example of construction of a driving apparatus according to this eighth embodiment. In Fig. 68, the components having the same functions as those in Fig. 67, are denoted by the same references as those in Fig. 67, respectively. Thus the repetitive descriptions thereof will be omitted.

[0399] In the construction shown in Fig. 68, the driver circuit 51' on the scanning electrode Y side is made as part of an LSI such as a scan driver circuits. Besides, the switch SW8 connected to the power supply line of the voltage Vx' and the switch SW9' connected to the power supply line of the voltage Vw are provided on the common electrode X side and the scanning electrode Y side, respectively. On the scanning electrode Y side, the transistors Tr22 and Tr23 are omitted.

[0400] Fig. 69 is a timing chart showing driving waveforms of the PDP by the driving apparatus constructed as shown in Fig. 68. Fig. 69 shows one of the subfields making up one frame. The waveforms shown in Fig. 69 is almost the same as the waveforms shown in Fig. 64. These waveforms are generated by controlling ON/OFF of the switches SW1 to SW5, SW8, SW1' to SW3', and SW9', which are provided in common for all display lines, and the switches SW4' and SW5' in the scan driver 51' for a display line i, at proper timings.

[0401] In either of the constructions shown in Figs. 67 and 68, the area for mounting circuit parts can be considerably reduced. This makes it possible to realize a small device and a reduced cost in manufacturing.

[0402] In the examples of Figs. 67 and 68, both the switches SW4' and SW5' are disposed at such positions as shown in the first embodiment, i.e., within the driver circuit. Alternatively, the switch SW4' can be disposed at such a position as shown in the second embodiment, i.e., within the power supply circuit. Or, the switch SW5' can be disposed at such a position as shown in the third embodiment, i.e., within the power supply circuit. The switch SW5' in the second embodiment or the switch SW4' in the third embodiment can be constructed by an LSI such as a scan driver circuit.

[0403] In this case, even in the driver circuit with an LSI structure by a scan driver, the switch necessary for each display line may be either the switch SW4' or SW5'. Thus the total number of switches can be considerably decreased, thereby reducing the circuit scale and cost.

(Ninth Embodiment)

[0404] Next, the ninth embodiment of the present invention will be described. In this ninth embodiment, the driver circuit on either side for applying voltages to a load 20, i.e., either of the driver circuits on the common electrode X side and the scanning electrode Y side is made as part of an LSI such as a scan driver circuit.

[0405] Fig. 70 is a circuit diagram showing a specific example of construction of a driving apparatus according to this ninth embodiment. In Fig. 70, the components having the same functions as those in Fig. 9 or 67, are denoted by the same references as those in Fig. 9 or 67, respectively. Thus the repetitive descriptions thereof will be omitted.

[0406] Referring to Fig. 70, the driver circuit 51 on the common electrode X side is made as part of an LSI such as a scan driver circuit. That is, unlike the power supply circuit 43, which is a common circuit for all display lines provided in the PDP, such a driver circuit 51 is provided for every display line. Namely, there are provided the same numbers of switches SW4 and SW5 as the number of display lines.

[0407] Also the driver circuit 51' on the scanning electrode Y side is made as part of an LSI such as a scan driver circuit. That is, unlike the power supply circuit 43', which is a common circuit for all display lines provided in the PDP, such a driver circuit 51' is provided for every display line. Namely, there are provided the same numbers of switches SW4' and SW5' as the number of display lines.

[0408] In this construction, in both of the common electrode X side and the scanning electrode Y side, by switching control of the switches SW4, SW5, SW4', and SW5' provided for each display line, in the sustain discharge period, the voltage to be applied to the display line can be controlled individually. Besides, on the scanning electrode Y side, the transistors Tr22 and Tr23 in the above-described embodiments, which are the switching elements for applying the voltage (-Vs/2) in the address period, can be omitted.

[0409] Fig. 71 is a circuit diagram showing another example of construction of a driving apparatus according to this ninth embodiment. In Fig. 71, the components having the same functions as those in Fig. 70 or 63, are denoted by the same references as those in Fig. 70 or 63, respectively. Thus the repetitive descriptions thereof will be omitted.

[0410] In the construction shown in Fig. 71, the driver circuits 51 and 51' on the common electrode X side and the scanning electrode Y side are respectively made as parts of LSIs such as scan driver circuits. Besides, the switch SW8 connected to the power supply line of the

side and the scanning electrode Y side in reset period can be controlled properly.

[0424] Fig. 74 is a timing chart showing driving waveforms of the PDP by the driving apparatus constructed as shown in Fig. 73. Fig. 74 shows one of the subfields making up one frame. Fig. 74 also shows a state that the voltage Vw is applied by making control of a switch (not shown in Fig. 73), which is exclusively used for the voltage. The basic forms of the driving waveforms shown in Fig. 74 are the same as those in Fig. 49, which were already described, but the amplitudes are different.

[0425] According to the timing chart of Fig. 74, the breakdown voltages of the elements provided in the power supply circuit 43 and the driver circuit 44 on the common electrode X side can respectively be Vs/3 + Vw and Vs/3, so the breakdown voltage can be held down in comparison with the value in previously-considered apparatus. Besides, the breakdown voltages of the elements provided in the power supply circuit 43' and the driver circuit 44' on the scanning electrode Y side can respectively be 2Vs/3 + Vw and 2Vs/3, so the breakdown voltage can be held down in comparison with the value in previously-considered apparatus also on this side.

[0426] Fig. 75 is a circuit diagram showing another example of construction of a driving apparatus according to this tenth embodiment. In Fig. 75, the components having the same functions as those in Fig. 73, are denoted by the same references as those in Fig. 73, respectively. Thus the repetitive descriptions thereof will be omitted.

[0427] In this example of Fig. 75, the voltages V2 and V1 to be applied to the power supply circuits 43' and 43 on the scanning electrode Y side and the common electrode X side are kVs and lVs, respectively (V1 + V2 = nVs). The other features are quite the same as those in Fig. 73. For example, when it is wanted to apply a high voltage between the common and scanning electrodes X and Y in order to improve the luminescence efficiency of a gas discharge, it is also possible that V1 = V2 = Vs (V1 + V2 = 2Vs). In this case, with each element in the driving apparatus having the same breakdown voltage as in previously-considered apparatus, a higher difference voltage can be applied between the common and scanning electrodes X and Y.

[0428] In PDP, the voltage Vs to be applied between the common and scanning electrodes X and Y in sustain discharge period, is 150 to 190 V in general. This voltage is determined by the kind of gas charged within the PDP, the material of electrodes, the gap between the common and scanning electrodes X and Y, etc. The display luminance of PDP is determined by how many times the voltage Vs is applied between the common and scanning electrodes X and Y in sustain discharge period to make a gas discharge occur. The power required for a gas discharge in applying the voltage Vs each time is determined by the kind of gas, the material of electrodes, the gap between the electrodes, etc., as described above. The ratio of the luminance to a unit of power is called luminescence efficiency.

[0429] In PDP, there is a request to obtain a high luminance with a little power. If the kind of gas, the material of electrodes, the gap between the electrodes, etc., are selected in order to meet the request, i.e., for increasing the luminescence efficiency, the voltage Vs becomes high. As a result, the breakdown voltage of the circuit becomes high, resulting in a high cost. Contrastingly, according to this embodiment, without raising the breakdown voltage, the high voltage can be applied with the same breakdown voltage as in previously-considered apparatus, and the luminescence efficiency can be increased.

(Eleventh Embodiment)

[0430] Next, the eleventh embodiment of the present invention will be described. This eleventh embodiment is to give specific examples of the above tenth embodiment, in which V1 = 0 and V2 = Vs, or V1 = Vs and V2 = 0, and the driving waveforms in the sustain discharge period are applied through one of the common and scanning electrodes X and Y.

[0431] Fig. 76 is a circuit diagram showing a specific example of construction of a driving apparatus according to this eleventh embodiment. In Fig. 76, the components having the same functions as those in Fig. 48, are denoted by the same references as those in Fig. 48, respectively. Thus the repetitive descriptions thereof will be omitted. The example of Fig. 76 differs from the example of Fig. 48 only in the feature that the power supply voltage to which the switches SW1 and SW1' are connected, is Vs in Fig. 76 though it is Vs/2 in Fig. 48.

[0432] Fig. 77 is a timing chart showing an example of driving waveforms in a sustain discharge period by the driving apparatus shown in Fig. 76. In this example of Fig. 77, the driving waveforms on the common electrode X side is the same as those shown in Fig. 50 except the feature that the level of the voltage to be swung is Vs. Thus the repetitive description will be omitted.

[0433] On the scanning electrode Y side, the switches SW1', SW3', and SW5' are kept ON, and the switches SW2' and SW4' and the transistors Tr15 and Tr16 in the power recovery circuit 33 are kept OFF all during the execution of the series of switching operations on the common electrode X side. The voltage being applied to the scanning electrode Y is thereby always kept at zero (the ground level) through the switch SW3'. Alternatively, the reverse manner can also be employed in which the switches SW2' and SW4' are kept ON and the switches SW1', SW3', and SW5' are kept OFF to keep the voltage being applied to the scanning electrode Y at zero.

[0434] In this manner, when the voltage on the scanning electrode Y side is fixed to the ground level, and Vs is used as a power supply voltage for the common

and 80, are denoted by the same references as those in Figs. 78 and 80, respectively. Thus the repetitive descriptions thereof will be omitted.

[0448] In this driving apparatus shown in Fig. 82, the common electrode X side of the load 20 is connected to the power supply line for a voltage Vax through a switch 21, and grounded through a switch SW22. By turning one of the switches SW21 and SW22, the voltage to be applied to the common electrode X can be changed over between the ground level and Vax to use.

[0449] Fig. 83 is a timing chart showing driving waveforms of the PDP by the driving apparatus constructed as shown in Fig. 82. In this example of Fig. 83, the waveforms of the scanning and address electrodes Y and A are quite the same as those in Figs. 79 and 81. One of the ground level and Vax is applied to the common electrode X by being switched. More specifically, the voltage being applied to the common electrode X is fixed at the ground level during reset and sustain discharge periods, and at Vax during address period.

[0450] Fig. 84 is a circuit diagram showing still another example of construction of a driving apparatus according to this eleventh embodiment. In the above examples of Figs. 78, 80, and 82, the voltage being applied to the common electrode X is fixed at the ground level or Vax. But in the driving apparatus shown in Fig. 84, the voltage on the common electrode X side is not fixed, and various voltages may be applied at need. For this purpose, on the common electrode X side, a switch SW9 for switching operation in relation to the power supply line for a voltage Vw', and a switch SW14 for switching operation in relation to the power supply line for a voltage Vax, are connected in parallel to the second signal line OUTB.

[0451] On the scanning line Y side, a switch SW18 is connected between the scan driver 31' and the power supply line for a voltage Vsc, and a switch SW19 is connected between the scan driver 31' and the power supply line for a voltage (-Vy). Both terminals of the scan driver 31' are respectively connected to switches SW23 and SW 24. The node between those switches SW23 and SW 24 is grounded.

[0452] Fig. 85 is a timing chart showing driving waveforms of the PDP by the driving apparatus constructed as shown in Fig. 84. Fig. 85 shows one of the subfields making up one frame. Referring to Fig. 85, on the common electrode X side, by ON/OFF control of the switches SW1 to SW5, SW9, and SW 14 at proper timings, pulses of various voltages, e.g., Vw' and Vax necessary in reset and address periods, other than the voltages (±Vs) in sustain discharge period, are applied to the load 20.

[0453] On the scanning electrode Y side, during reset and sustain discharge periods, by setting either of the switches SW18 and SW19 OFF, and either of the switches SW23 and SW24 ON, the voltage being applied is fixed at the ground level. In address period, by keeping the switches SW23 and SW24 OFF. By turning the switches SW18 and SW19 ON, the voltage Vsc - (-Vy) is applied between both power supply terminals of the scan driver 31'. By controlling ON/OFF of the scan driver 31' at proper timings, a pulse voltage necessary for scanning is applied to the scanning electrode Y. With this construction, the circuit on the scanning electrode Y side can be further simplified, so it can be realized to reduce the manufacturing cost in comparison with the prior art.

[0454] The address electrode A is fixed at the ground level during any period but address period in which the voltage Va is applied. During sustain discharge period, the address electrode A may be kept in a high impedance state.

[0455] Fig. 86 is a circuit diagram showing still another example of construction of a driving apparatus according to this eleventh embodiment. In Fig. 86, the components having the same functions as those in Fig. 84, are denoted by the same references as those in Fig. 84, respectively. Thus the repetitive descriptions thereof will be omitted. In the above example of Fig. 84, the switches SW23 and SW24 for setting the voltage being applied to the scanning electrode Y, at the ground level, are constructed as a common circuit for all display lines of the PDP.

[0456] Contrastingly in the construction shown in Fig. 86, a switch 25 for setting the voltage being applied to the scanning electrode Y, at the ground level, is incorporated in the scan driver 31' as part of the scan driver 31'. Such a switch 25 is provided for every display line. By this construction, switching control can be individually made for each display line. Besides, the circuit on the scanning electrode Y side can be further simplified, so it can be realized to reduce the manufacturing cost in comparison with the prior art. The waveforms in this construction of Fig. 86 is the same as those of Fig. 85.

(Twelfth Embodiment)

[0457] Next, the twelfth embodiment of the present invention will be described.

[0458] In the above-described first to eleventh embodiment, a positive voltage is applied to the power supply circuit, and positive and negative voltages are generated on the first and second signal lines OUTA and OUTB from the positive voltage. Contrastingly in this twelfth embodiment, a negative voltage is applied to the power supply circuit, and positive and negative voltages are generated on the output line OUTC through the first and second signal lines OUTA and OUTB from the negative voltage.

[0459] Fig. 87 is a circuit diagram showing a specific example of construction of a driving apparatus according to this twelfth embodiment. In Fig. 87, the components having the same functions as those in Fig. 9, are denoted by the same references as those in Fig. 9, respectively. Thus the repetitive descriptions thereof will be omitted. The example of Fig. 87 differs from the example of Fig. 9 on the point that the voltage to be applied

in the capacitors C1 and C7. Further, by turning the respective switches SW5 and SW4 OFF and ON, the voltage (Vs/4) of the first signal line OUTA is output on the output line OUTC to be applied to the common electrode X of the load 20.

[0473] Next, the switches SW26, SW27, SW28, and SW4 are set ON, and the remaining switches SW1, SW2, SW3, and SW5 are set OFF. With this operation, the capacitors C1 and C7 are connected in series between the ground and the power supply line of the voltage (1/4Vs). Since the charges corresponding to the voltage (1/4Vs) are stored in the capacitors C1 and C7, the charges in the capacitors C1 and C7 are summed to generate the voltage of (Vs/2) of the first signal line OUTA. Even in this state, the voltage of the second signal line OUTB still remains at the ground level. At this time, since the respective switches SW5 and SW4 are OFF and ON, the voltage (Vs/2) of the first signal line OUTA is output on the output line OUTC to be applied to the common electrode X of the load 20.

[0474] At the next timing, the switches SW1, SW3, SW27, SW28, and SW4 are set ON, and the remaining switches SW2, SW26, and SW5 are set OFF. The voltage (Vs/4) is thereby applied to the first signal line OUTA through the switch SW1. In this state, the voltage of the second signal line OUTB remains at the ground level. At this time, since the respective switches SW5 and SW4 are OFF and ON, the voltage (Vs/4) of the first signal line OUTA is output on the output line OUTC to be applied to the common electrode X of the load 20.

[0475] Next, the switches SW4 and SW5 are turned OFF and ON, respectively. The voltage of the second signal line OUTB is thereby output on the output line OUTC to set the voltage being applied to the common electrode X of the load 20 at the ground level.

[0476] After this, the switches SW3, SW26, and SW5 are turned ON, the remaining switches SW1, SW2, SW27, SW28, and SW4 are turned OFF. The voltage of the second signal line OUTB is thereby lowered to (-Vs/4) in accordance with the charges accumulated in the capacitor C7. At this time, since the switch SW5 is ON, the voltage (-Vs/4) of the second signal line OUTB is output on the output line OUTC to be applied to the common electrode X of the load 20.

[0477] Next, the switches SW3 and SW2 are turned OFF and ON, respectively. This makes the state that the capacitors C1 and C7 are connected in series between the common electrode X and the ground. At this time, since the charges corresponding to (Vs/4) are accumulated in either of the capacitors C1 and C7, the voltage of the second signal line OUTB is lowered to (-Vs/2) as a result of addition of the charges in those two capacitors C1 and C7. The voltage of the first signal line OUTA remains at the ground level. At this time, since the switch SW5 is ON, the voltage (-Vs/2) of the second signal line OUTB is output on the output line OUTC to be applied to the common electrode X of the load 20.

[0478] After this, the switches SW2 and SW3 are again turned OFF and ON, respectively. By this operation, the voltage of the first signal line OUTA is raised to (+Vs/4), and the voltage of the second signal line OUTB is lowered to (-Vs/4). At this time, since the switch SW5 is ON, the voltage (-Vs/4) of the second signal line OUTB is output on the output line OUTC to be applied to the common electrode X of the load 20.

[0479] Next, similarly to the first state, five switches SW1, SW3, SW27, SW28, and SW5 are turned ON, and the remaining switches SW2, SW26, and SW4 are turned OFF. The voltage of the first signal line OUTA is set at (Vs/4), and the voltage of the second signal line OUTB is set at the ground level. At this time, the voltage of the second signal line OUTB is output on the output line OUTC to be applied to the common electrode X of the load 20. After this, the same operation is repeated.

[0480] Although not shown in Fig. 91, a similar switching control to that on the common electrode X side is performed in relation to the switches SW1', SW2', SW3', SW26', SW27', SW28', SW4', and SW5' on the scanning electrode Y side. But, as shown in Fig. 91, the switching control is performed such that the output voltages of the output lines OUTC and OUTC' on the common electrode X side and the scanning electrode Y side are reverse in polarity to each other.

[0481] As described above, according to this embodiment, the waveforms in which the positive and negative voltages (±Vs/2) are alternately repeated, can be generated on the output lines OUTC and OUTC' with a single power supply for generating the voltage (Vs/4). By applying the positive and negative voltages (±Vs/2) thus generated are applied in opposite phases to the output lines OUTC and OUTC' on the common electrode X side and the scanning electrode Y side, the difference voltage (Vs) can be applied between the common and scanning electrodes X and Y of the load 20.

[0482] As described above, when driving the capacitive load 20, the power is expressed by $2Cp \cdot V^2 \cdot f$ using the capacitance Cp of the load 20, the driving voltage V of the load 20, and the frequency when the voltage is applied to the load 20. According to this embodiment, the absolute value of the voltage to be applied to the load 20 suffices to be 1/4 the conventional one. Instead of this, however, the frequency when the voltage is applied to the load 20 becomes four times. Consequently, the power loss when driving the load 20 is expressed by $2Cp \cdot (V/4)^2 \cdot (4f)$. This shows that the power loss can be held down to 1/4 the conventional one. Thus, even in case of providing no power supply circuit, the power use efficiency can be improved in comparison with the prior art.

[0483] In this example, the positive and negative voltages (±Vs/2) are applied in opposite phases between the common and scanning electrodes X and Y. But, for example, the positive and negative voltages (±Vs) may be applied to the common electrode X while the scanning electrode Y side is connected to the ground, like the eleventh embodiment. In this case, the construction

voltages (±Vs/2) thus generated are applied in opposite phases to the output lines OUTC and OUTC' on the common electrode X side and the scanning electrode Y side, the difference voltage (Vs) can be applied between the common and scanning electrodes X and Y of the load 20. In this manner, since the absolute value of the voltage to be applied to the load 20 suffices to be 1/4 the conventional one, the power loss can be held down to 1/4 the conventional one. Thus, even in case of providing no power recovery circuit, the power use efficiency can be improved in comparison with the prior art.

[0496] For setting the voltage of the output line OUTC (OUTC') at the ground level, a method is thinkable in which the voltages of the first and second signal lines OUTA (OUTA') and OUTB (OUTB') are respectively set at the ground level and (-Vs/4), and then the switch SW4 (SW4') is turned ON. However, in order to obtain longer periods for charging the capacitors C1, C7, C4, and C8, the example shown in Fig. 94 is preferable.

[0497] In this example, the positive and negative voltages (±Vs/2) are applied in opposite phases between the common and scanning electrodes X and Y. But, for example, the positive and negative voltages (±Vs) may be applied to the common electrode X while the scanning electrode Y side is connected to the ground, like the eleventh embodiment. In this case, the construction shown in Fig. 96 can be used. In the construction shown in Fig. 96, the construction on the common electrode X side is almost the same as that shown in Fig. 94 except the feature that the power supply line is not of (Vs/4) but of (Vs/2). In the construction shown in Fig. 96, the scanning electrode Y side is connected to the ground. The driving waveforms in this case are as shown in Fig. 97.

[0498] As described above, according to the example of Fig. 96, the waveforms in which the positive and negative voltages (±Vs) are alternately repeated, can be generated on the output lines OUTC and OUTC' with a single power supply for generating the voltage (Vs/2).

[0499] In the example of Fig. 94, the driving waveforms are generated with an A/D power supply of the voltage (Vs/4). But, by further adding, in series, low-voltage and low-power power supply circuit sections each having the same construction as the switches SW26 to SW28 and the capacitor C7 as shown in Fig. 94, the same driving waveforms can be generated with an A/D power supply of a smaller voltage (e.g., Vs/8, Vs/16, ...). Thus the power loss when driving the load 20 can be reduced more. For example, when n stages of such low-voltage and low-power power supply circuit sections are provided in series, the power loss when driving the load 20 is expressed by $2Cp\cdot(V/n)^2\cdot(nf)$. This shows that the power loss can be held down to 1/n the conventional one.

[0500] Fig. 98 is a circuit diagram showing another example of construction of a driving apparatus according to this thirteenth embodiment. In Fig. 98, the components having the same functions as those in Figs. 96 and 84, are denoted by the same references as those in Figs. 96 and 84, respectively. Thus the repetitive descriptions thereof will be omitted.

[0501] In the driving apparatus shown in Fig. 98, combined are the feature that two stages of low-voltage and low-power circuit sections are provided in series on the common electrode X side as shown in the example of Fig. 96, the feature that the negative voltage (-Vs/2) is used as a power supply as shown in Fig. 87, and the feature that the scanning electrode Y side is made up from the scan driver 31' and the power supply line of the voltage Vsc, and the voltages (±Vs) are applied to one side of the load 20, as shown in Fig. 84.

[0502] This construction makes it possible to apply the voltages (±Vs) to the load 20 from the common electrode X side, thereby simplifying the circuit construction on the scanning electrode Y side. Besides, the external power supply voltage is (-Vs/2), and the power loss in relation to the load 20 becomes half that of previously-considered apparatus. Further, the breakdown voltage of either of the driver circuit 44 and the scan driver 31' is sufficed by Vs/2 or more (in case of Vsc = Vs/2). This shows that the breakdown voltage can be held down to half the value in previously-considered apparatus.

[0503] Fig. 99 is a timing chart showing a specific example of driving waveforms in sustain discharge period by the driving apparatus shown in Fig. 98.

[0504] Referring to Fig. 99, the driving waveforms of the output lines OUTC and OUTC' on the common electrode X side and the scanning electrode Y side are quite the same as those shown in Fig. 97. In the example of Fig. 97, the duration of either of the driving waveforms of the first and second signal lines OUTA and OUTB on the common electrode X side in the period of the (Vs/2) level is longer than that in the period of the ground level. This relation is reverse in the example of Fig. 99, i.e. the duration thereof in the period of the ground level is longer than that in the period of the (Vs/2) level. The other features of the waveforms in both drawings are almost the same.

[0505] For setting the voltage of the output line OUTC at the ground level, a method is thinkable in which the voltages of the first and second signal lines OUTA and OUTB are respectively set at (Vs/2) and the ground level, and then the switch SW5 is turned ON. However, in order to obtain longer periods for charging the capacitors C1 and C7, the example shown in Fig. 99 is preferable, in which the voltages of the first and second signal lines OUTA and OUTB are respectively set at the ground level and (-Vs/2), and then the switch SW4 is turned ON.

[0506] Besides, for setting the voltages of the first and second signal lines OUTA and OUTB respectively at (Vs/2) and the ground level, the switches SW1 and SW30 are turned ON in the example of Fig. 99. Alternatively, the switches SW2 and SW28 may be turned ON. Further, when the switch SW27 is also turned ON, the charges accumulated in the capacitor C1 can be more efficiently used.

[0507] The first to thirteenth embodiments of the

Claims

1. A driving apparatus for applying predetermined voltages to a load,

   said apparatus comprising a first signal line for supplying a voltage at a first level to one side of said load, and a second signal line for supplying a voltage at a second level to said one side of said load,

   wherein the voltage of said second signal line is set at a third level and the voltage of said first signal line is set at said first level so that the voltage at said first level is supplied to said load through said first signal line, and

   the voltage of said first signal line is set at said third level and the voltage of said second signal line is set at said second level so that the voltage at said second level is supplied to said load through said second signal line.

2. An apparatus according to claim 1, further comprising a driving circuit provided between said first and second signal lines for driving said load, wherein said driving circuit selectively applies the voltage at said first level given through said first signal line and the voltage at said second level given through said second signal line to said one side of said load.

3. An apparatus according to claim 1, wherein said third level is the ground level.

4. An apparatus according to claim 1, wherein the other side of said load is connected to a fixed power supply or the ground.

5. An apparatus according to claim 1, wherein the other side of said load is connected through a switching element to a fixed power supply or the ground.

6. An apparatus according to claim 1, wherein said load is a plasma display panel, and the other side of said load is connected to a fixed power supply through a scan driver circuit for generating a pulse to be applied in address period, and a switching element.

7. An apparatus according to claim 6, wherein said scan driver circuit is connected also to the ground through a switching element.

8. An apparatus according to claim 7, wherein said switching element connected to the ground is provided within said scan driver circuit.

9. An apparatus according to claim 1, wherein a power supply for generating a positive voltage in relation to said third level is used for supplying the voltages at said first, second, and third levels to said first and second signal lines.

10. An apparatus according to claim 1, wherein a power supply for generating a negative voltage in relation to said third level is used for supplying the voltages at said first, second, and third levels to said first and second signal lines.

11. An apparatus according to claim 1, further comprising a third signal line for supplying a voltage at a fourth level to the other side of said load, and a fourth signal line for supplying a voltage at a fifth level to said other side of said load,

    wherein the voltage of said fourth signal line is set at a sixth level and the voltage of said third signal line is set at said fourth level so that the voltage at said fourth level is supplied to said load through said third signal line, and

    the voltage of said third signal line is set at said sixth level and the voltage of said fourth signal line is set at said fifth level so that the voltage at said fifth level is supplied to said load through said fourth signal line.

12. An apparatus according to claim 11, wherein the voltage at said fifth level is supplied to said other side of said load through said fourth signal line while the voltage at said first level is supplied to said one side of said load through said first signal line, and

    the voltage at said fourth level is supplied to said other side of said load through said third signal line while the voltage at said second level is supplied to said one side of said load through said second signal line, thereby applying said predetermined voltage to said load.

13. An apparatus according to claim 11, wherein said first and second levels are respectively equal to said fourth and fifth levels, said third and sixth levels are respectively the ground level, and a common power supply for generating the voltage at said first and fourth or second and fifth level on both sides of said load is provided.

14. An apparatus according to claim 11, wherein said first and second levels are different from said fourth and fifth levels, respectively.

15. An apparatus according to claim 14, wherein either said first or second level, and either said fourth or fifth level are respectively the ground level.

16. An apparatus according to claim 11, wherein a power supply for generating a positive voltage in relation to said sixth level is used for supplying the voltages at said fourth, fifth, and sixth levels to said third and fourth signal lines.

29. An apparatus according to claim 27, further comprising:

sixth and seventh switches connected in series between a third power supply for supplying the voltage at said fourth or fifth level, and a fourth power supply for supplying the voltage at said sixth level;
a capacitor whose one terminal is connected to the node between said sixth and seventh switches; and
an eighth switch connected between the other terminal of said capacitor and said fourth power supply,

wherein said third and fourth signal lines are connected to both terminals of said capacitor, and
said third and fourth signal lines are connected to said other side of said load.

30. An apparatus according to claim 29, further comprising:
ninth and tenth switches connected in series between said third and fourth signal lines connected to both terminals of said capacitor,
wherein the node between said ninth and tenth switches is connected to said other side of said load.

31. An apparatus according to claim 28, wherein said fourth switch is turned ON after said first switch is turned ON.

32. An apparatus according to claim 28, wherein said first switch is turned ON after said fourth switch is turned ON.

33. An apparatus according to claim 27, wherein each of said first to third switches is made up from a MOSFET and a diode connected to said MOSFET.

34. An apparatus according to claim 27, wherein said first switch is made up from a p- or n-channel MOSFET connected to said first power supply, and a diode whose anode is connected to the drain or source of said p- or n-channel MOSFET.

35. An apparatus according to claim 27, wherein said second switch is made up from an n-channel MOSFET connected to said second power supply, and a diode whose cathode is connected to the drain of said n-channel MOSFET.

36. An apparatus according to claim 27, wherein said third switch is made up into two sets of a MOSFET and a diode connected to said MOSFET, said two sets being connected to each other.

37. An apparatus according to claim 28, wherein control of said first to fifth switches is performed in accordance with a program recorded in a recording medium.

38. An apparatus according to claim 1, further comprising:

first, fourth, and second switches connected in series between a first power supply for supplying the voltage at said first or second level, and a second power supply for supplying the voltage at said third level;
a capacitor whose one terminal is connected to the node between said fourth and second switches;
a third switch connected between the other terminal of said capacitor and said second power supply; and
a fifth switch connected between said first signal line connected to the node between said first and fourth switches, and said second signal line connected to said other terminal of said capacitor,

wherein said load is connected to the node between said first signal line and said fifth switch.

39. An apparatus according to claim 1, further comprising:

first and second switches connected in series between a first power supply for supplying the voltage at said first or second level, and a second power supply for supplying the voltage at said third level;
a capacitor whose one terminal is connected to the node between said first and second switches;
fifth and third switches connected in series between the other terminal of said capacitor and said second power supply; and
a fourth switch connected between said first signal line connected to said one terminal of said capacitor, and said second signal line connected to the node between said fifth and third switches,

wherein said load is connected to the node between said fourth switch and said second signal line.

40. An apparatus according to claim 27, further comprising an offset circuit for generating an offset voltage on said first and second signal lines.

41. An apparatus according to claim 29, further comprising a circuit for supplying a voltage other than

level in sustain period.

62. An apparatus according to claim 11, wherein said load is a line-sequential scan type and memory type plasma display panel in which scanning electrodes and common electrodes are alternately disposed,

said apparatus further comprises:

an odd number common electrode driver for driving the common electrodes in odd numbers, and an even number common electrode driver for driving the common electrodes in even numbers; and

an odd number scanning electrode driver for driving the scanning electrodes in odd numbers, and an even number scanning electrode driver for driving the scanning electrodes in even numbers,

either of said odd number and even number common electrode drivers comprises such first and second signal lines as defined above, and either of said odd number and even number scanning electrode drivers comprises such third and fourth signal lines as defined above,

said scanning and common electrodes are driven at a timing by the combination of said odd number common electrode driver and said odd number scanning electrode driver, and the combination of said even number common electrode driver and said even number scanning electrode driver, and at another timing by the combination of said odd number common electrode driver and said even number scanning electrode driver, and the combination of said even number common electrode driver and said odd number scanning electrode driver, and

voltages are thereby applied to said load with alternately switching the combinations of said drivers on the common electrode side and said drivers on the scanning electrode side.

63. A driving method for applying a predetermined voltage to a load,

wherein the voltage of a first signal line is changed between first and third levels, and the voltage of a second signal line is changed between said third level and a second level, and the voltage at said first level given by said first signal line in the state that the voltage of said second signal line is set at said third level, and the voltage at said second level given by said second signal line in the state that the voltage of said first signal line is set at said third level, are selectively applied to said load.

64. A plasma display apparatus comprising:

a plasma display panel;

first and second electrodes provided for applying a predetermined voltage to said plasma display panel to make a discharge occur; and

a driving circuit for driving said first and second electrodes,

wherein the first electrode side of said plasma display panel is provided with a first signal line for supplying a voltage at a first level to said first electrode, and a second signal line for supplying a voltage at a second level to said first electrode,

the voltage of said second signal line is set at a third level and the voltage of said first signal line is set at said first level so that the voltage at said first level is supplied to said first electrode through said first signal line,

the voltage of said first signal line is set at said third level and the voltage of said second signal line is set at said second level so that the voltage at said second level is supplied to said first electrode through said second signal line,

the second electrode side of said plasma display panel is provided with a third signal line for supplying a voltage at a fourth level to said second electrode, and a fourth signal line for supplying a voltage at a fifth level to said second electrode,

the voltage of said fourth signal line is set at a sixth level and the voltage of said third signal line is set at said fourth level so that the voltage at said fourth level is supplied to said second electrode through said third signal line, and

the voltage of said third signal line is set at said sixth level and the voltage of said fourth signal line is set at said fifth level so that the voltage at said fifth level is supplied to said second electrode through said fourth signal line.

65. A driving apparatus for applying predetermined voltages to a load,

said apparatus comprising a first signal line for supplying a voltage at a first level or a third level to one side of said load, and a second signal line for supplying a voltage at a second level or said third level to said one side of said load,

wherein the voltage of said second signal line is set at said third level and the voltage of said first signal line is set at said first level so that the voltage at said first level is supplied to said load through said first signal line, or the voltage at said third level is supplied to said load through said second signal line, and

the voltage of said first signal line is set at said third level and the voltage of said second signal line is set at said second level so that the voltage at said second level is supplied to said load through said second signal line, or the voltage at said third level

71. An apparatus according to claim 1, further comprising:

a transformer comprising a primary coil connected to a power supply for supplying the voltage at said first level, and a secondary coil;
a capacitor connected to both terminals of the secondary coil;
a first switch connected between a power supply for supplying the voltage at said third level, and one terminal of said secondary coil;
a second switch connected between said power supply for supplying the voltage at said third level, and the other terminal of said secondary coil; and
third and fourth switches connected in series between said first and second signal lines connected to both terminals of said capacitor,

wherein the node between said third and fourth switches is connected to said one side of said load.

72. A driving apparatus for applying a predetermined voltage to a load, said apparatus comprising:

first and second switches connected in series between a first power supply for supplying a voltage at a first level, and a second power supply for supplying a voltage at a third level;
a capacitor whose one terminal is connected to the node between said first and second switches;
a third switch connected between the other terminal of said capacitor and said second power supply;
a first signal line connected to said one terminal of said capacitor for outputting the voltage at said first level; and
a second signal line connected to said other terminal of said capacitor for outputting a voltage at a second level reverse in polarity to the voltage at said first level,

wherein the voltage at said first level given by said first signal line, and the voltage at said second level given by said second signal line are selectively applied to one side of said load.

73. A power supply circuit of a plasma display panel with at least a pair of electrodes for making a discharge occur, for applying a predetermined voltage to one of said electrodes, said circuit comprising:

a first signal line for outputting a voltage at a first level, and a second signal line for outputting a voltage at a second level,

wherein the voltage of said second signal line is set at a third level and the voltage of said first signal line is set at said first level to output the voltage at said first level through said first signal line, and

the voltage of said first signal line is set at said third level and the voltage of said second signal line is set at said second level to output the voltage at said second level through said second signal line.

74. A power supply circuit of a plasma display panel with at least a pair of electrodes for making a discharge occur, for applying a predetermined voltage to one of said electrodes, said circuit comprising:

first and second switches connected in series between a first power supply for supplying a voltage at a first level, and a second power supply for supplying a voltage at a third level;
a capacitor whose one terminal is connected to the node between said first and second switches;
a third switch connected between the other terminal of said capacitor and said second power supply;
a first signal line connected to said one terminal of said capacitor for outputting the voltage at said first level; and
a second signal line connected to said other terminal of said capacitor for outputting a voltage at a second level reverse in polarity to the voltage at said first level.

FIG. 2A

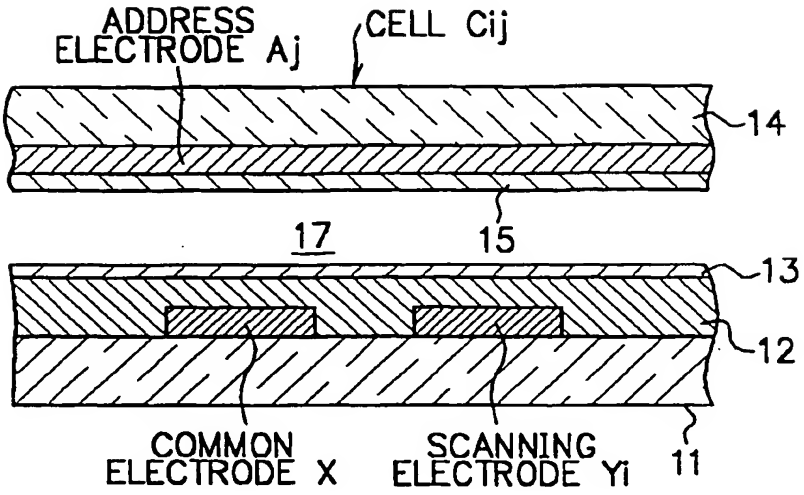


FIG. 2B

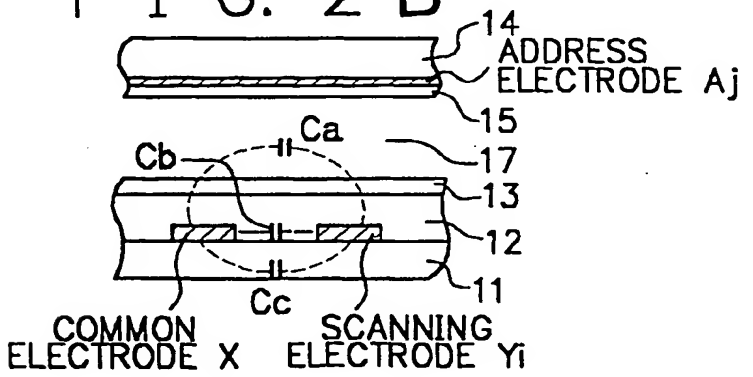


FIG. 2C

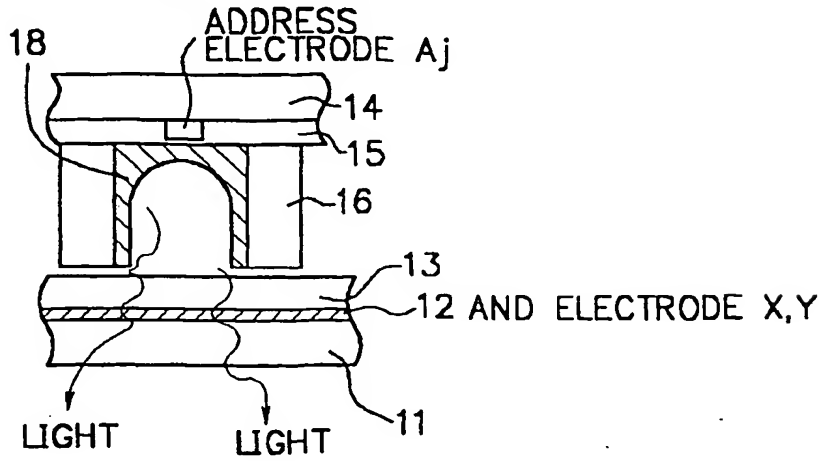


FIG. 4

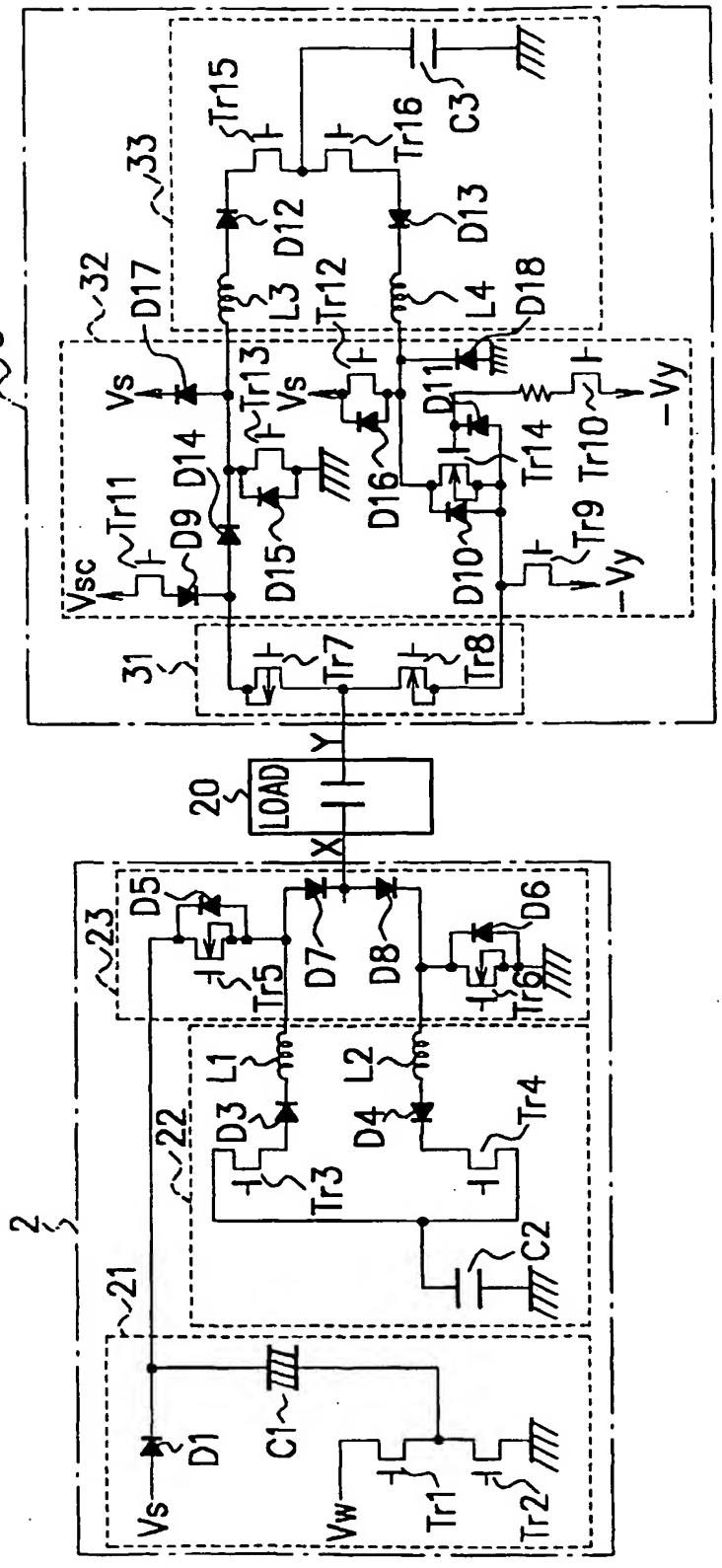

3
31
32
33
2
21
22
23
20
LOAD
X
Y
Vs
Vsc
Vw
-Vy
Tr1
Tr2
Tr3
Tr4
Tr5
Tr6
Tr7
Tr8
Tr9
Tr10
Tr11
Tr12
Tr13
Tr14
Tr15
Tr16
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
L1
L2
L3
L4
C1
C2
C3

FIG. 6

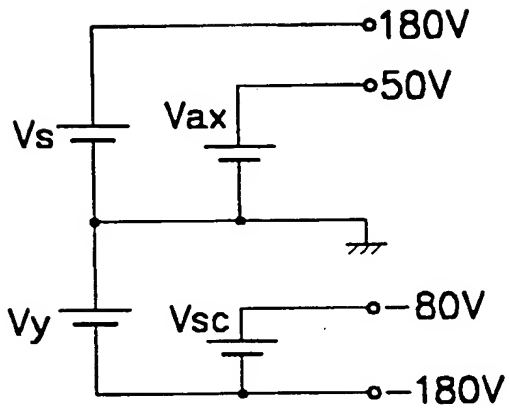


FIG. 8

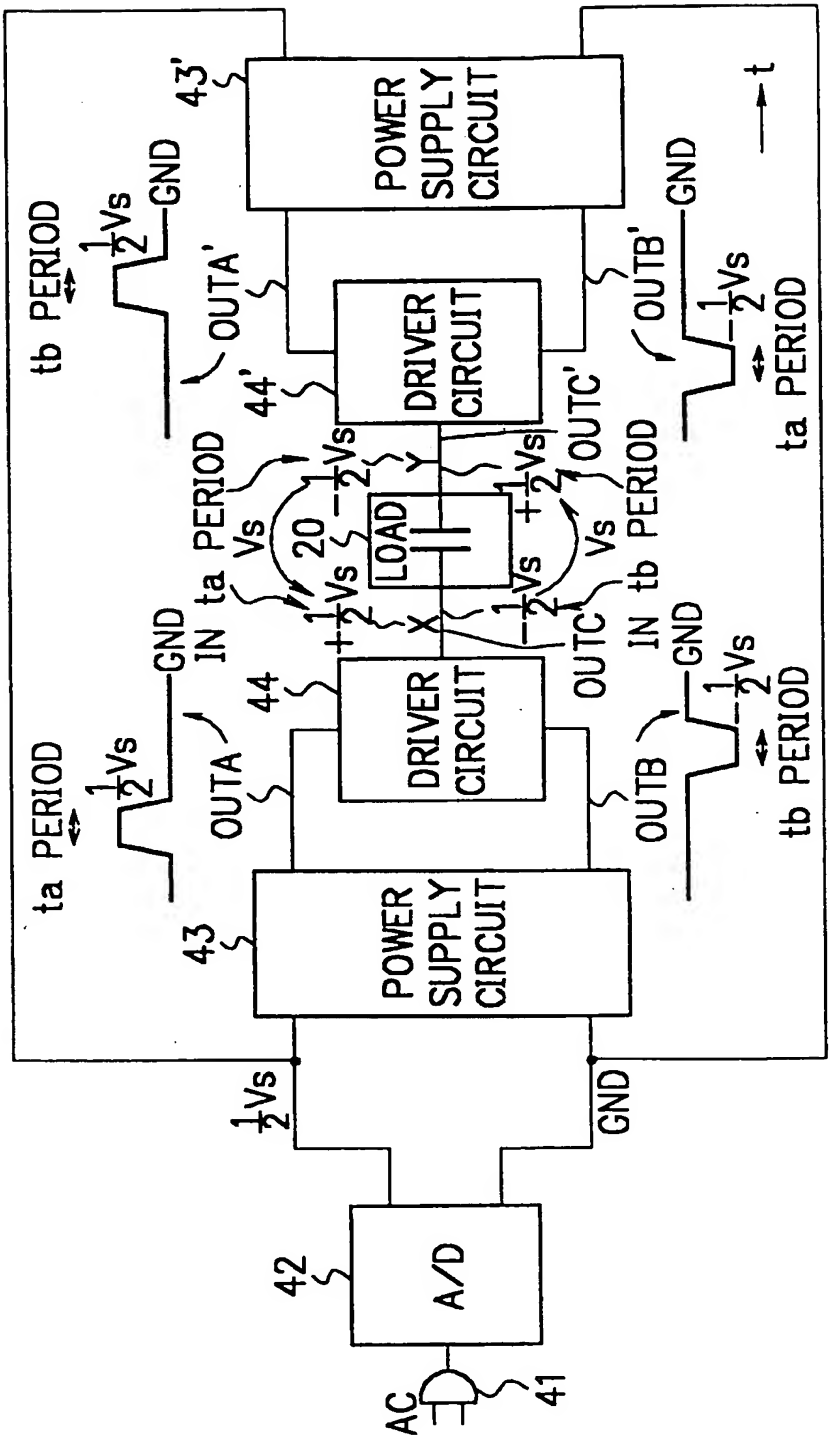

AC
41
42
A/D
43
POWER SUPPLY CIRCUIT
43'
POWER SUPPLY CIRCUIT
44
DRIVER CIRCUIT
44'
DRIVER CIRCUIT
LOAD
20
X
Y
OUTA
OUTB
OUTC
OUTA'
OUTB'
OUTC'
GND
1/2Vs
-1/2Vs
Vs
ta PERIOD
tb PERIOD
IN ta PERIOD
IN tb PERIOD
t

FIG. 10

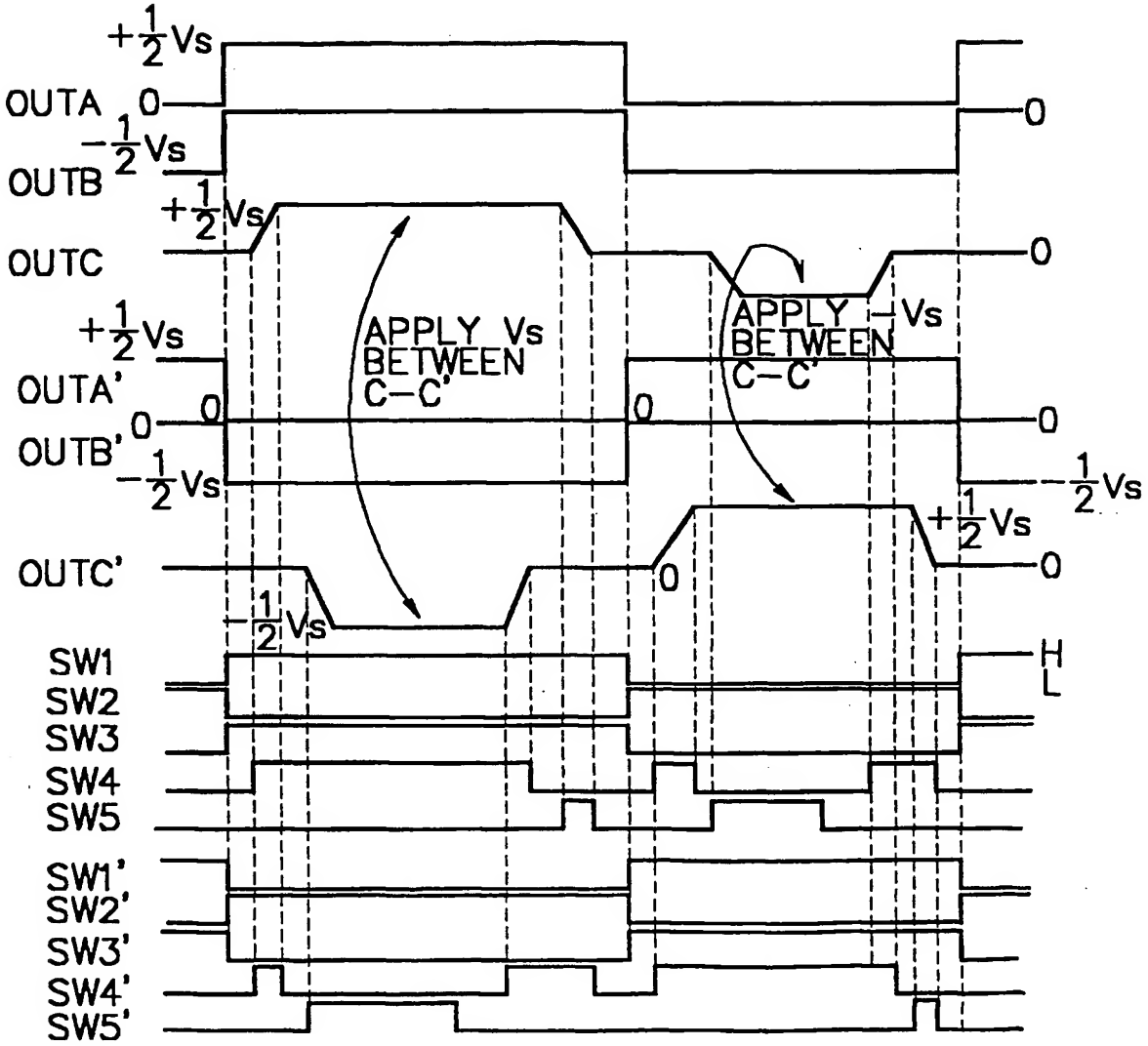

+1/2Vs
OUTA
0
−1/2Vs
OUTB
+1/2Vs
OUTC
+1/2Vs
OUTA'
0
OUTB'
−1/2Vs
OUTC'
−1/2Vs
APPLY Vs BETWEEN C−C'
APPLY −Vs BETWEEN C−C'
0
0
0
0
0
0
0
+1/2Vs
−1/2Vs
H
L
SW1
SW2
SW3
SW4
SW5
SW1'
SW2'
SW3'
SW4'
SW5'

FIG. 12

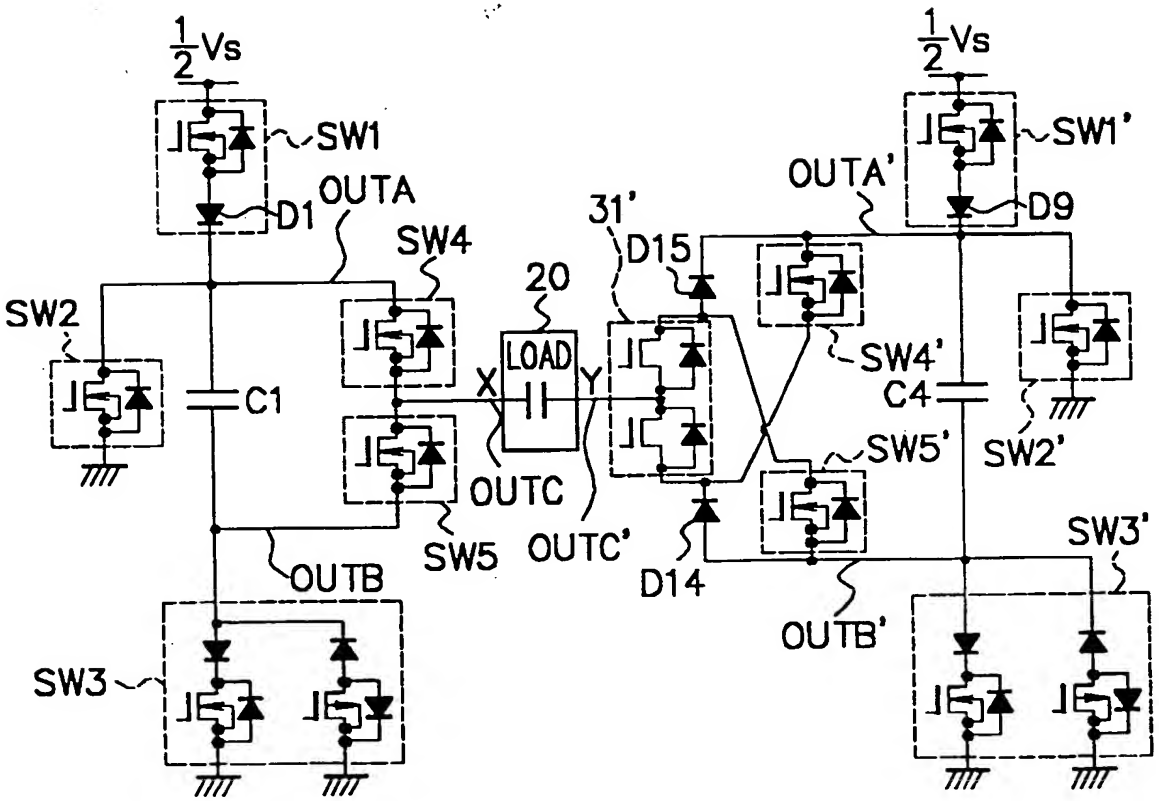

1/2Vs
SW1
D1
OUTA
SW4
SW2
C1
20
LOAD
X
Y
OUTC
SW5
OUTC'
OUTB
SW3
31'
D15
D14
1/2Vs
SW1'
OUTA'
D9
SW4'
C4
SW5'
SW2'
SW3'
OUTB'

FIG. 14

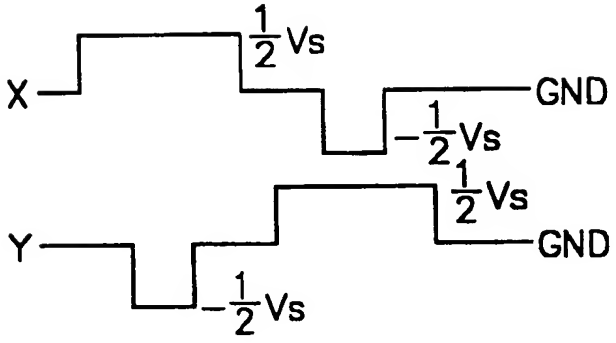


FIG. 15

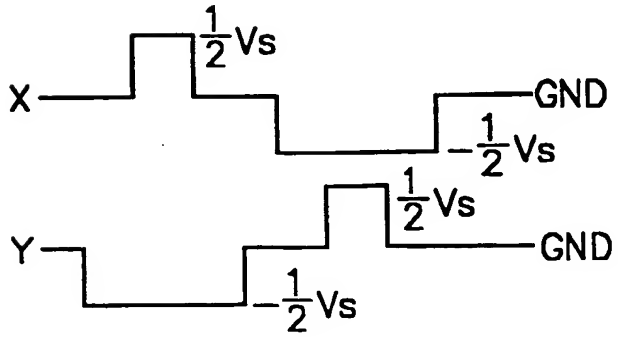


FIG. 18

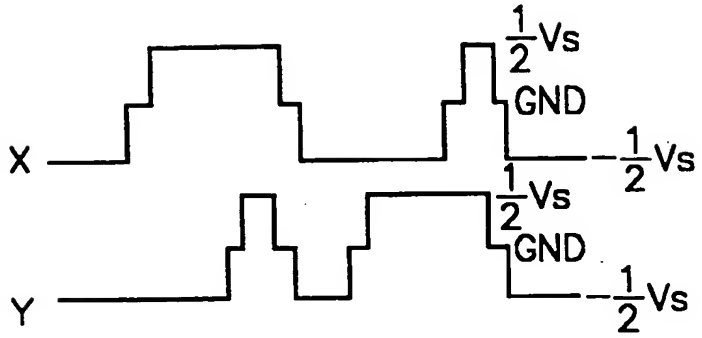
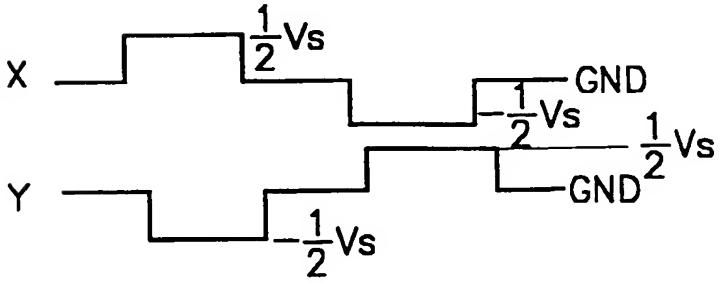


FIG. 19



F I G. 22

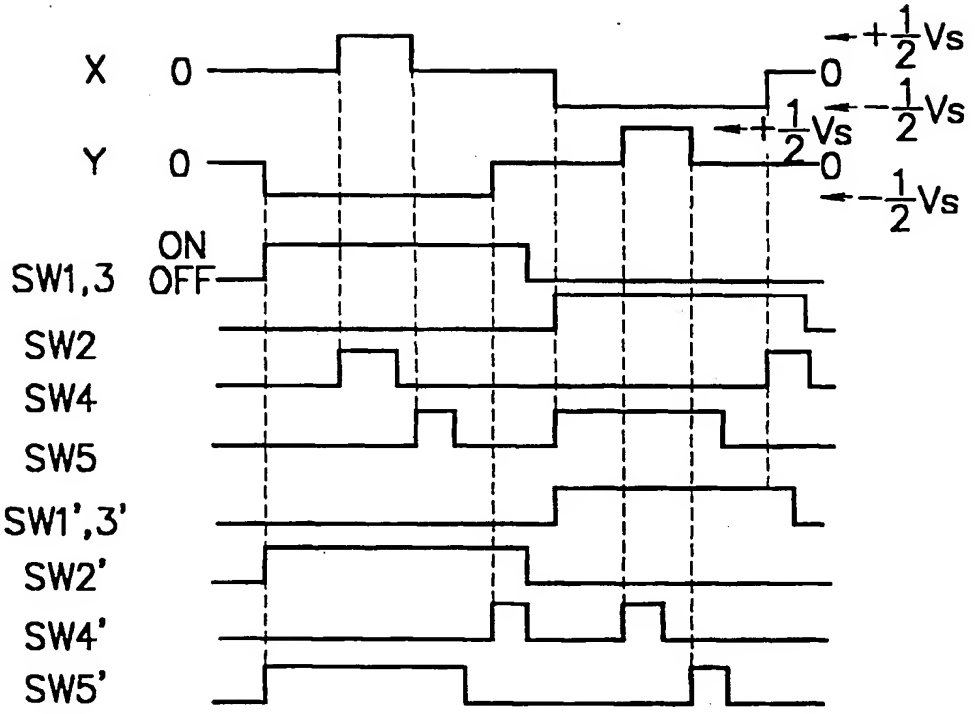

X
0
Y
0
ON
OFF
SW1,3
SW2
SW4
SW5
SW1',3'
SW2'
SW4'
SW5'
+1/2Vs
0
+1/2Vs
-1/2Vs
0
-1/2Vs

FIG. 24

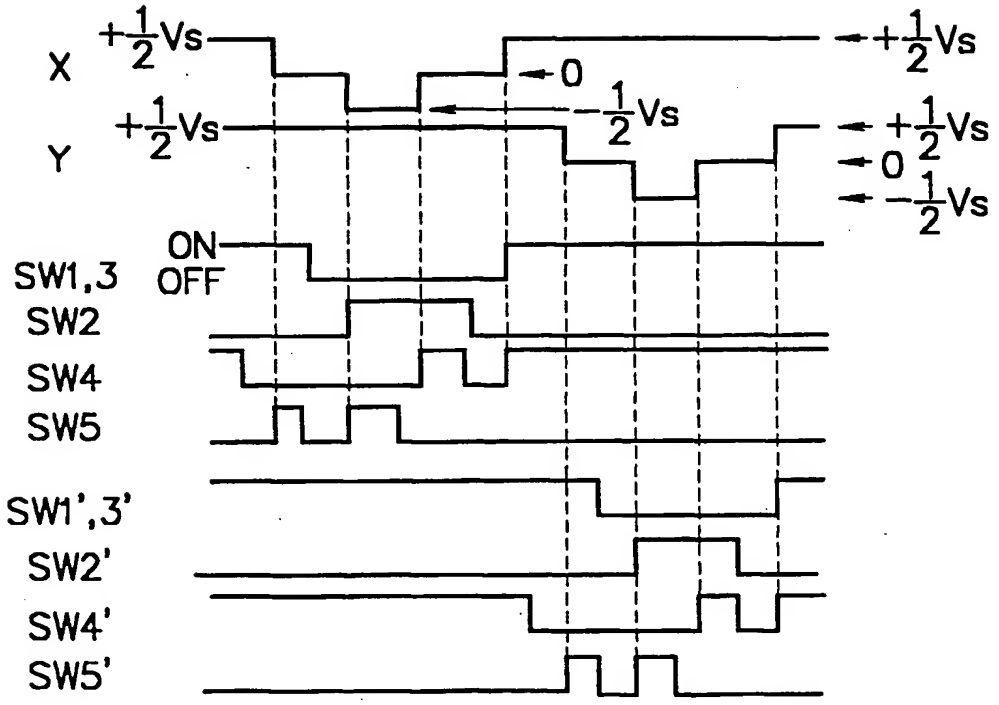

X
+1/2Vs
0
+1/2Vs
Y
+1/2Vs
-1/2Vs
+1/2Vs
0
-1/2Vs
SW1,3
ON
OFF
SW2
SW4
SW5
SW1',3'
SW2'
SW4'
SW5'

FIG. 26

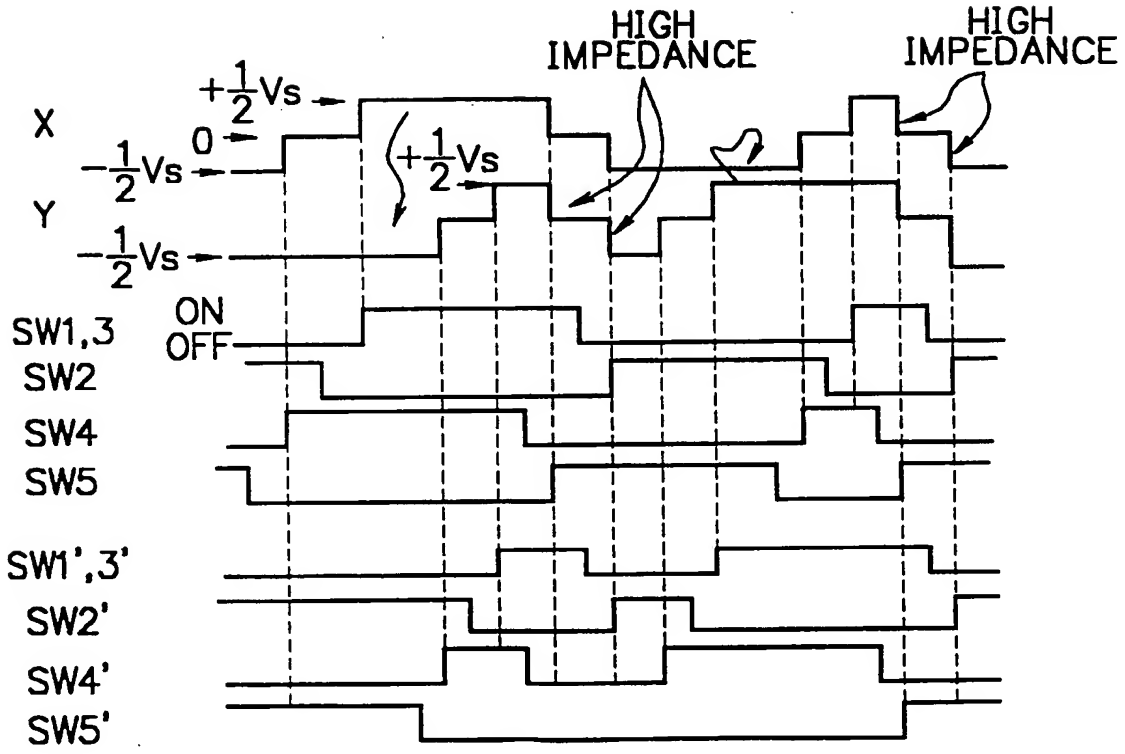

HIGH IMPEDANCE
HIGH IMPEDANCE
+1/2Vs
X
0
-1/2Vs
+1/2Vs
Y
-1/2Vs
ON
OFF
SW1,3
SW2
SW4
SW5
SW1',3'
SW2'
SW4'
SW5'

FIG. 28

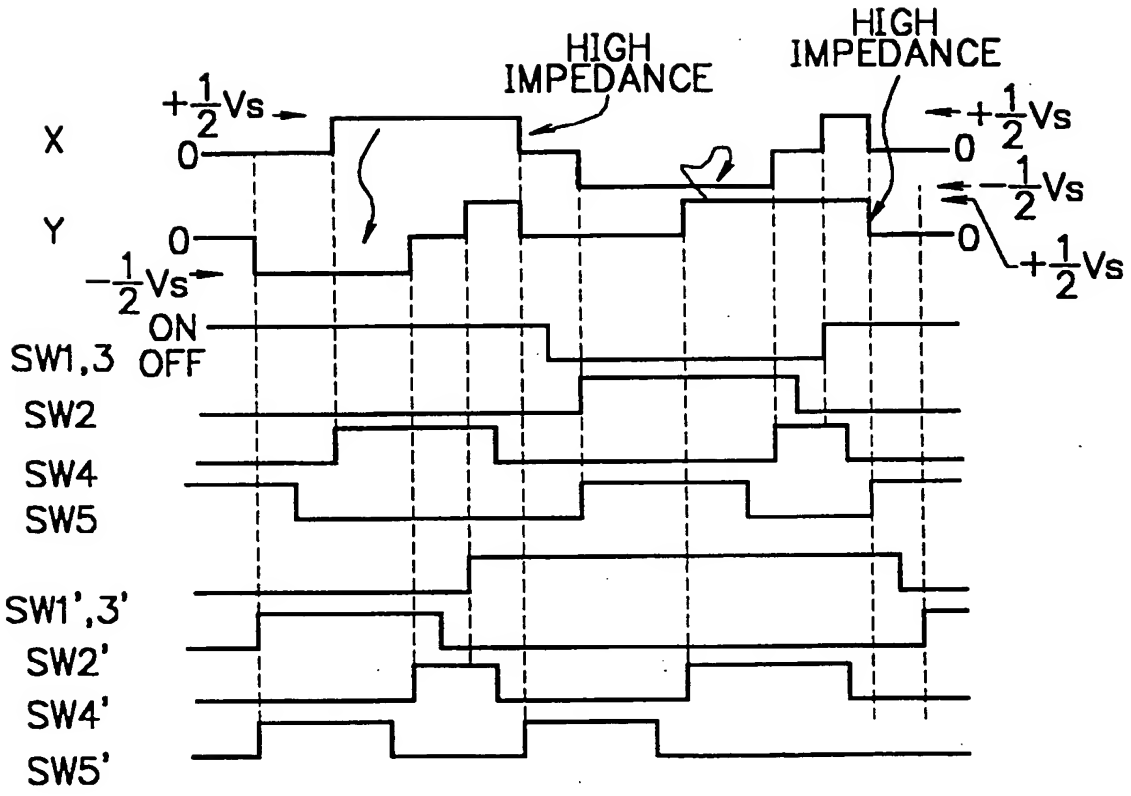

HIGH IMPEDANCE
HIGH IMPEDANCE
+1/2Vs
X
0
Y
0
-1/2Vs
+1/2Vs
0
-1/2Vs
0
+1/2Vs
ON
OFF
SW1,3
SW2
SW4
SW5
SW1',3'
SW2'
SW4'
SW5'

FIG. 30

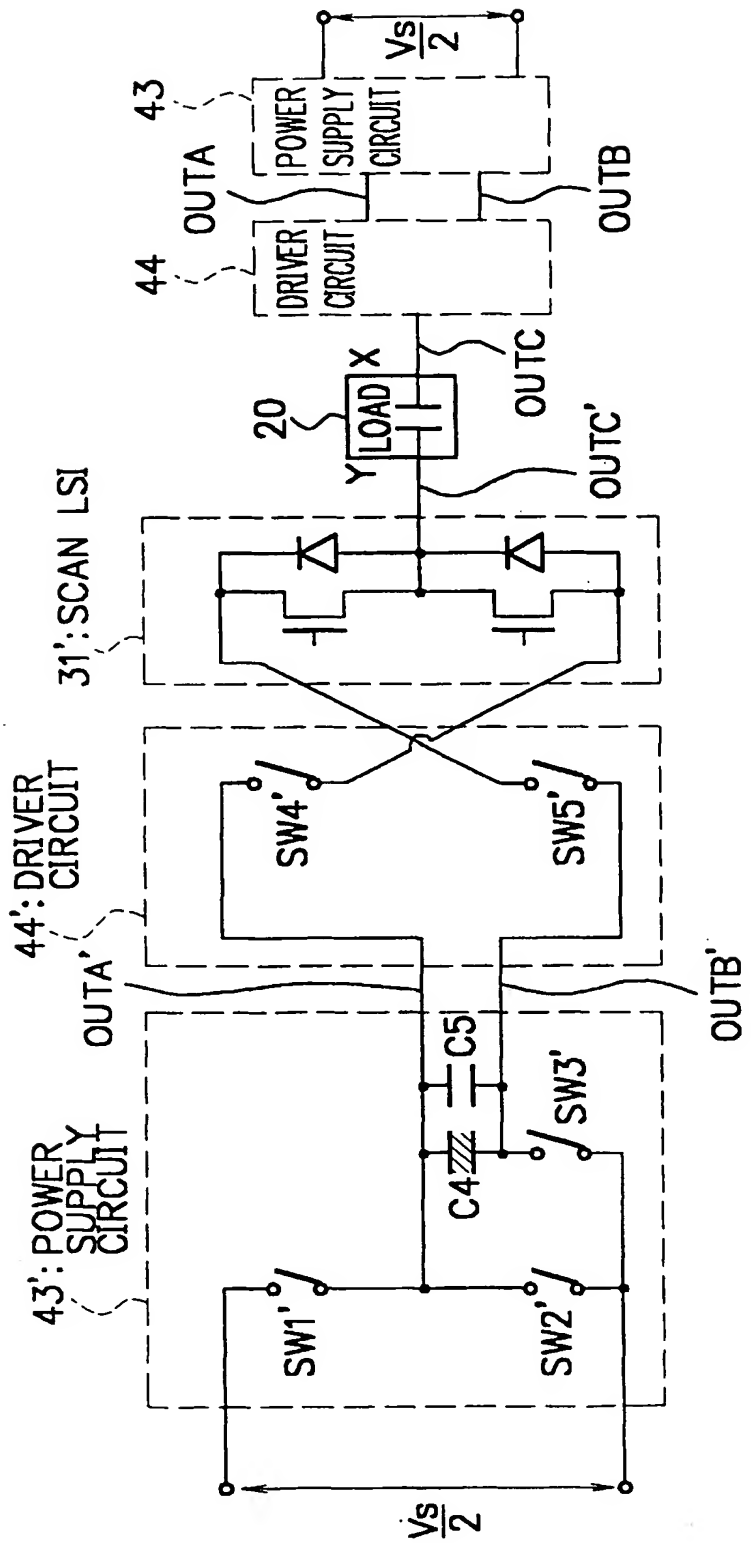

43
POWER SUPPLY CIRCUIT
Vs/2
OUTA
OUTB
44
DRIVER CIRCUIT
OUTC
20
X
LOAD
Y
OUTC'
31':SCAN LSI
44': DRIVER CIRCUIT
SW4'
SW5'
OUTA'
OUTB'
C5
C4
SW3'
43': POWER SUPPLY CIRCUIT
SW1'
SW2'
Vs/2

FIG. 33

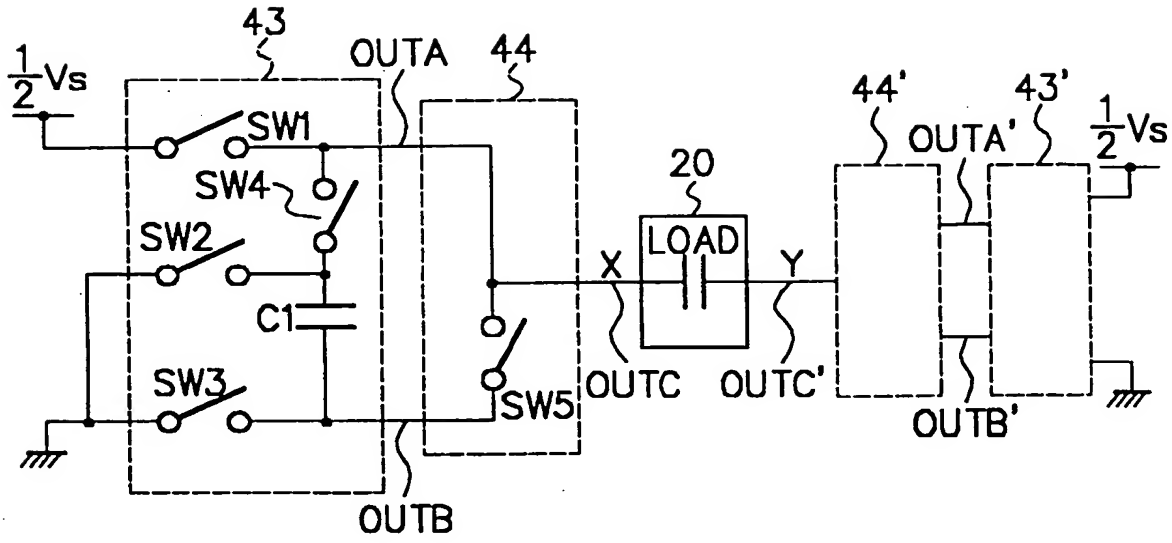

43
OUTA
44
1/2Vs
SW1
SW4
SW2
C1
SW3
SW5
OUTB
20
LOAD
X
Y
OUTC
OUTC'
44'
43'
OUTA'
1/2Vs
OUTB'

FIG. 35

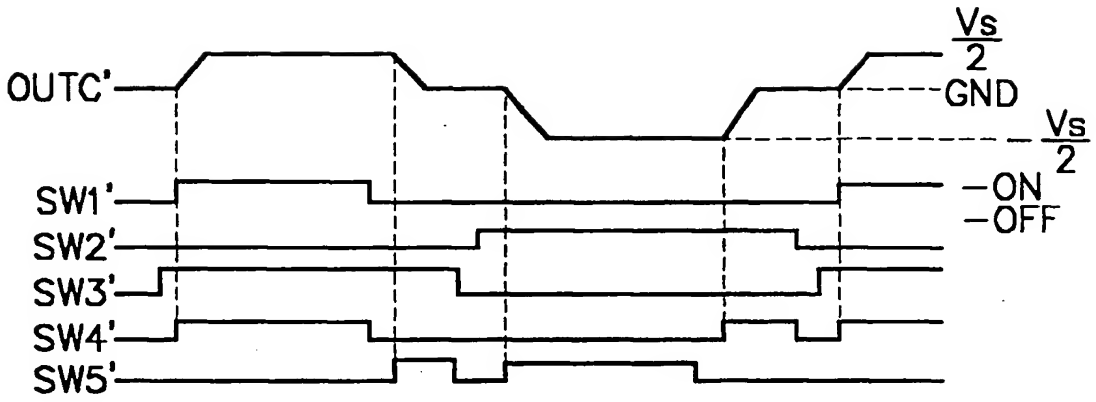


FIG. 37

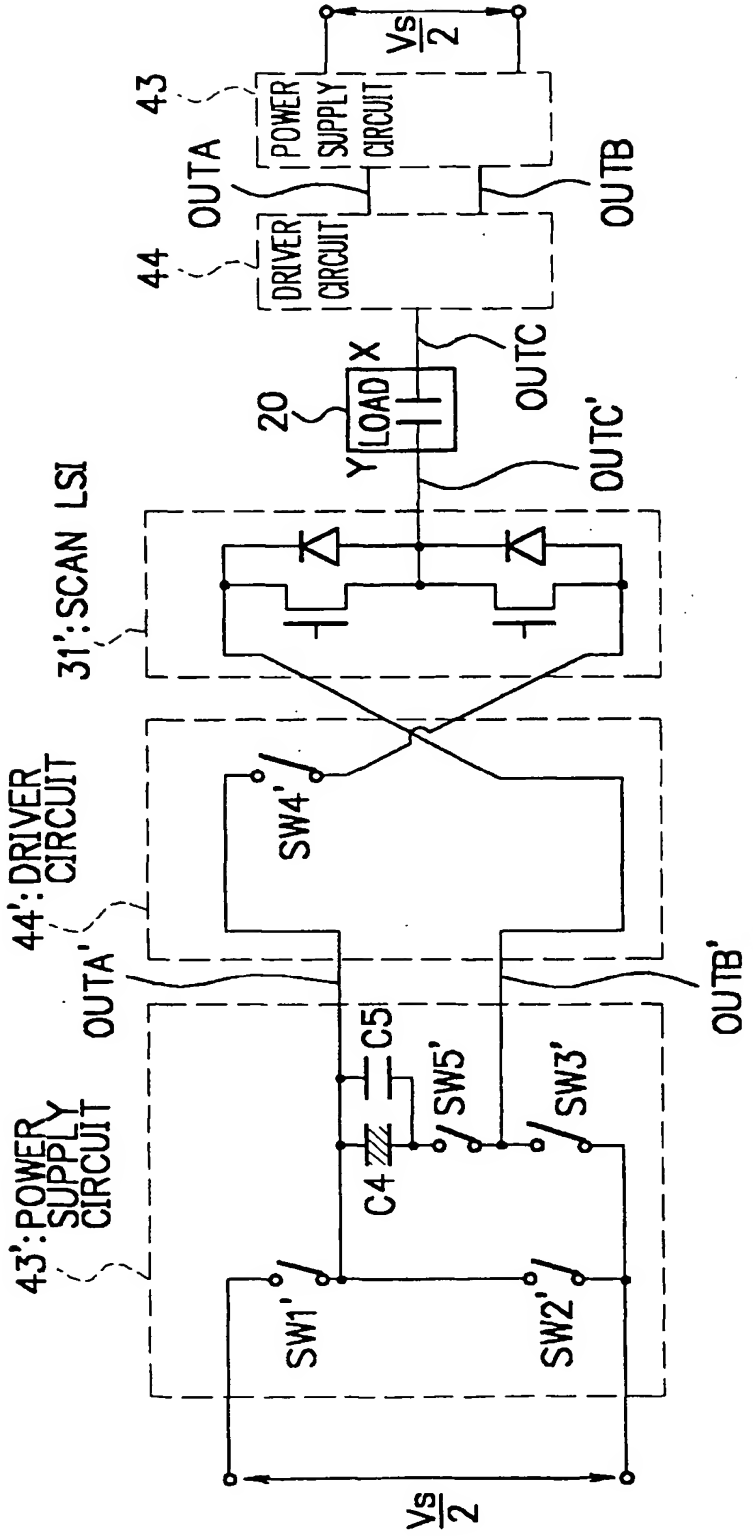

43
POWER SUPPLY CIRCUIT
Vs/2
OUTA
OUTB
44
DRIVER CIRCUIT
20
X
Y
LOAD
OUTC
OUTC'
31':SCAN LSI
44':DRIVER CIRCUIT
SW4'
OUTA'
OUTB'
43':POWER SUPPLY CIRCUIT
C5
C4
SW5'
SW3'
SW1'
SW2'
Vs/2

FIG. 39

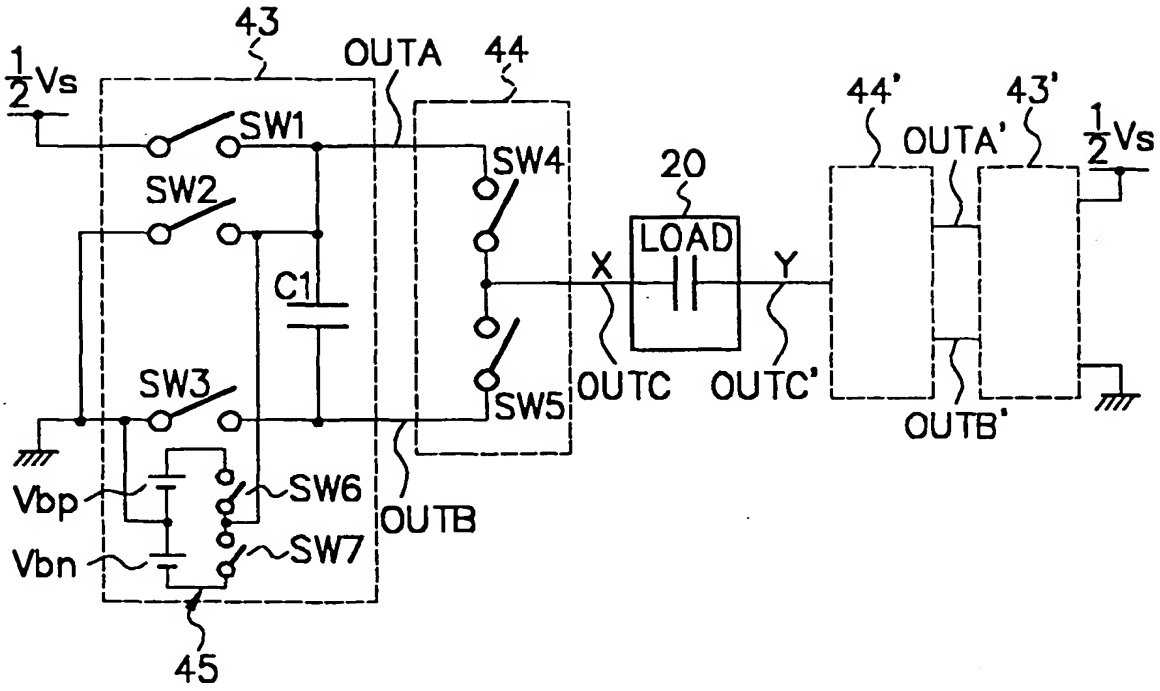

43
OUTA
44
1/2Vs
SW1
SW2
C1
SW3
SW4
SW5
20
LOAD
X
Y
OUTC
OUTC'
44'
43'
OUTA'
1/2Vs
OUTB'
Vbp
SW6
Vbn
SW7
OUTB
45

FIG. 41

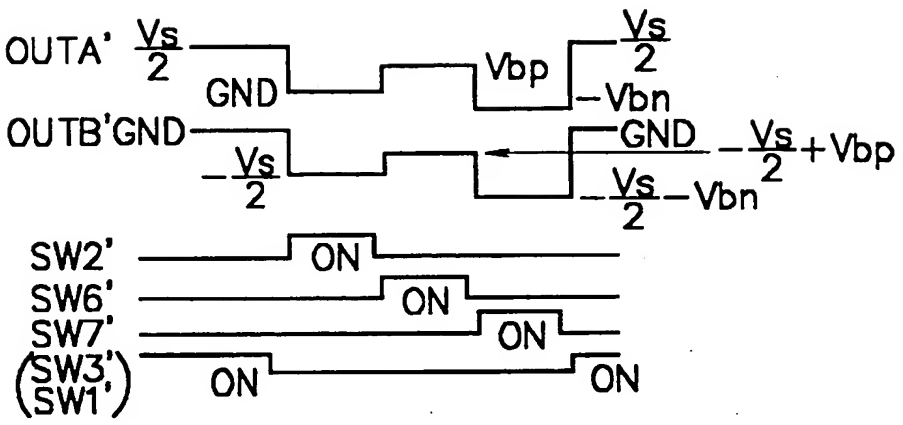

OUTA'
Vs/2
GND
Vbp
Vs/2
-Vbn
OUTB'GND
-Vs/2
GND
-Vs/2+Vbp
-Vs/2-Vbn
SW2'
ON
SW6'
ON
SW7'
ON
(SW3', SW1')
ON
ON

FIG. 43

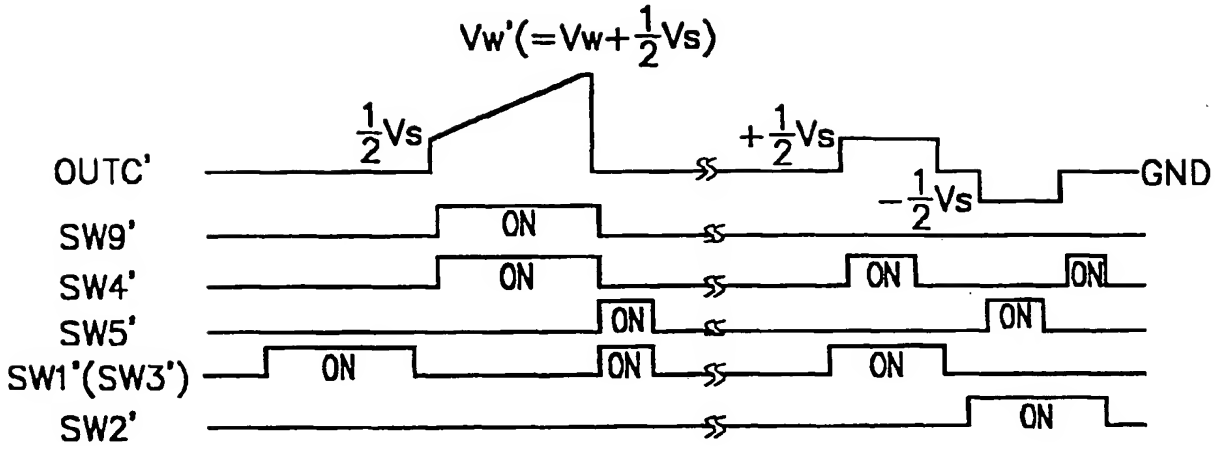


FIG. 45

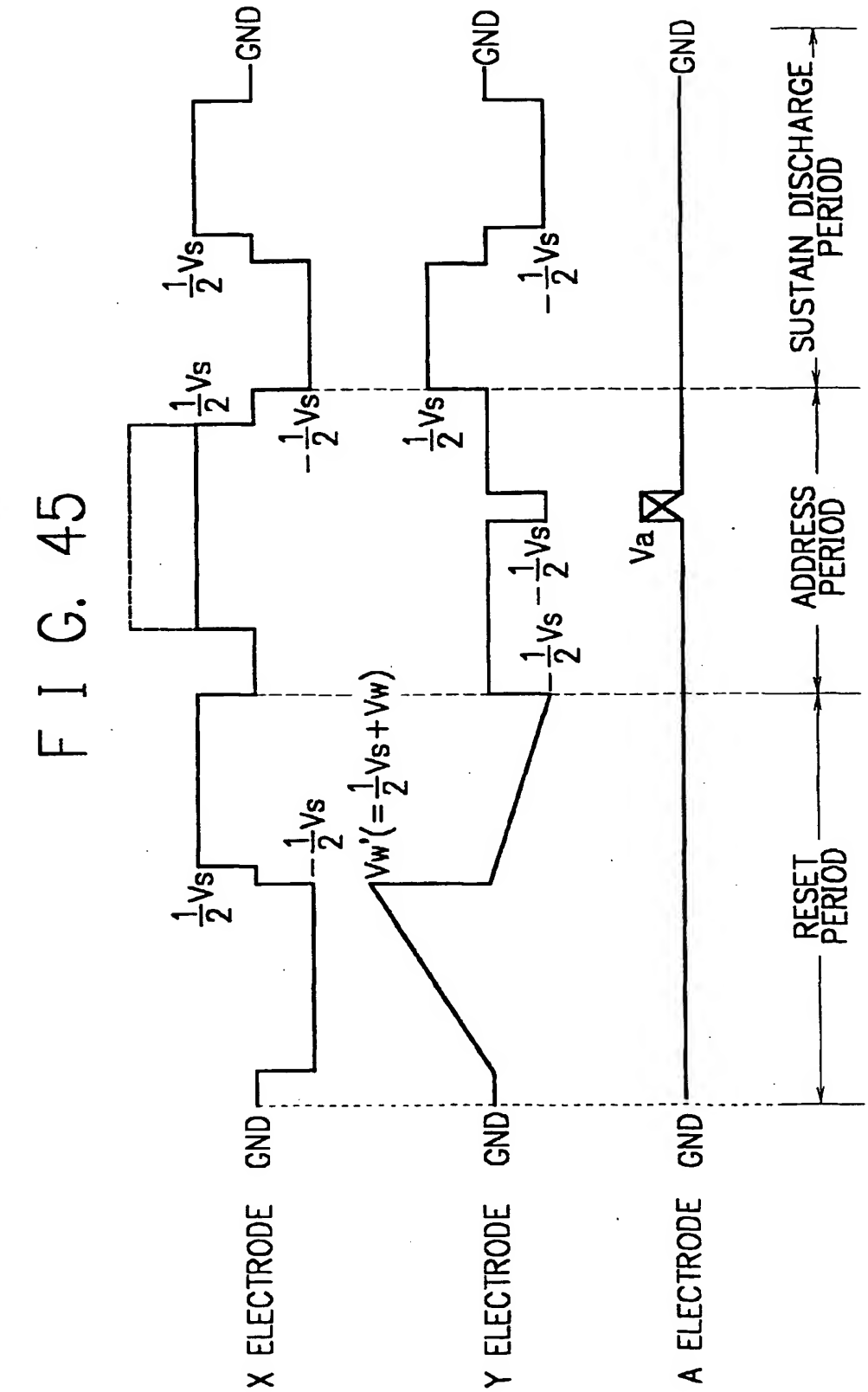

X ELECTRODE
Y ELECTRODE
A ELECTRODE
GND
GND
GND
$\frac{1}{2}$Vs
$-\frac{1}{2}$Vs
Vw'(=$\frac{1}{2}$Vs+Vw)
$\frac{1}{2}$Vs − $\frac{1}{2}$Vs
Va
RESET PERIOD
ADDRESS PERIOD
SUSTAIN DISCHARGE PERIOD

FIG. 47

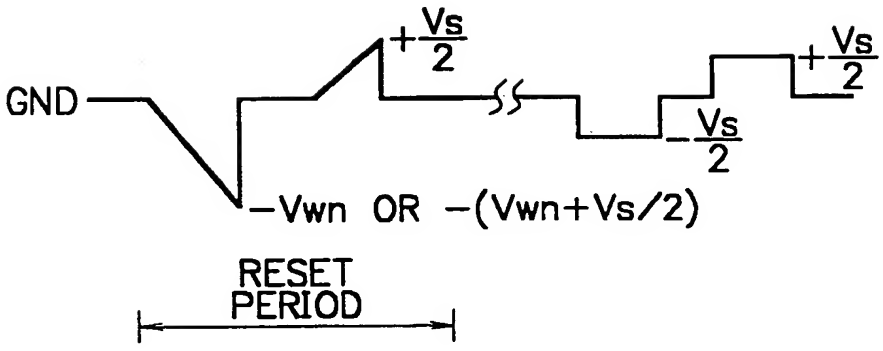


FIG. 49

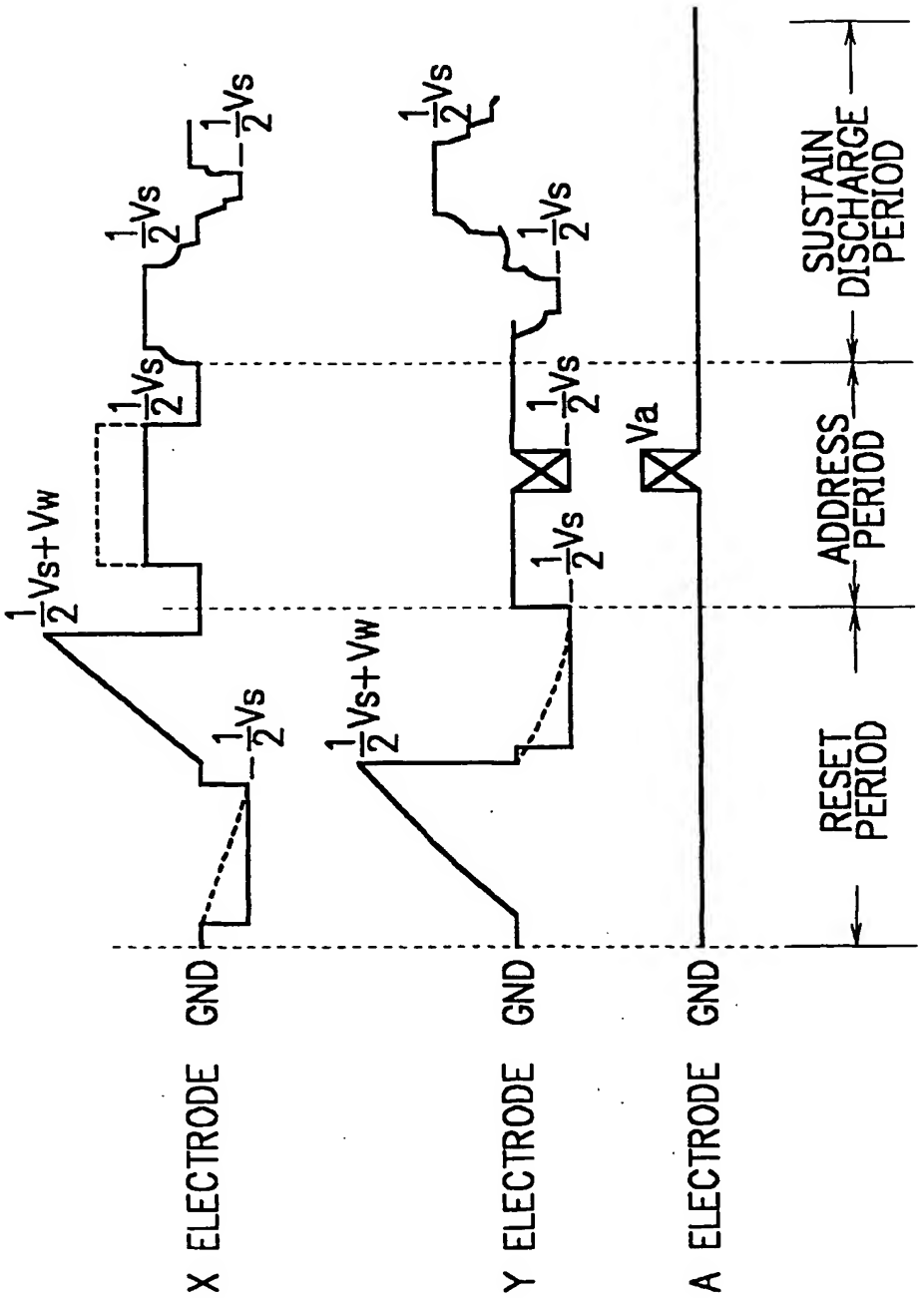

X ELECTRODE
Y ELECTRODE
A ELECTRODE
GND
GND
GND
1/2Vs+Vw
1/2Vs
1/2Vs
1/2Vs
1/2Vs
1/2Vs+Vw
1/2Vs
1/2Vs
1/2Vs
1/2Vs
Va
RESET PERIOD
ADDRESS PERIOD
SUSTAIN DISCHARGE PERIOD

FIG. 51

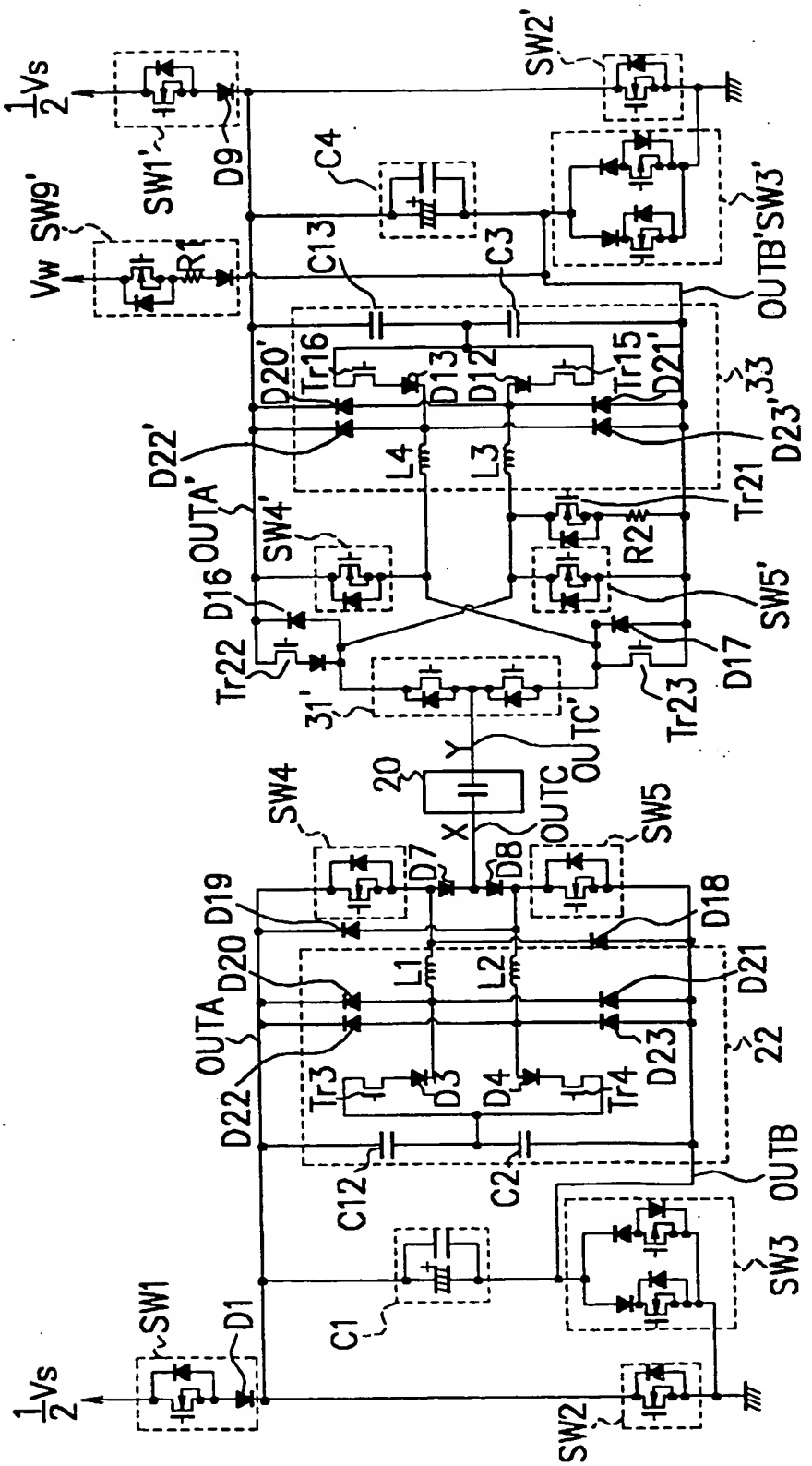

1/2Vs
SW1'
D9
SW2'
C4
SW9'
Vw
R1
C13
C3
OUTB'
SW3'
D20'
Tr16
D13
D12
Tr15
D21'
33'
D22'
L4
L3
D23'
OUTA'
SW4'
Tr21
R2
D16
SW5'
Tr22
D17
Tr23
31'
OUTC'
Y
20
X
OUTC
SW4
SW5
D7
D8
D19
D18
D20
L1
L2
D21
OUTA
22
D22
Tr3
D3
D4
Tr4
D23
C12
C2
OUTB
SW3
C1
SW1
D1
1/2Vs
SW2

FIG. 53

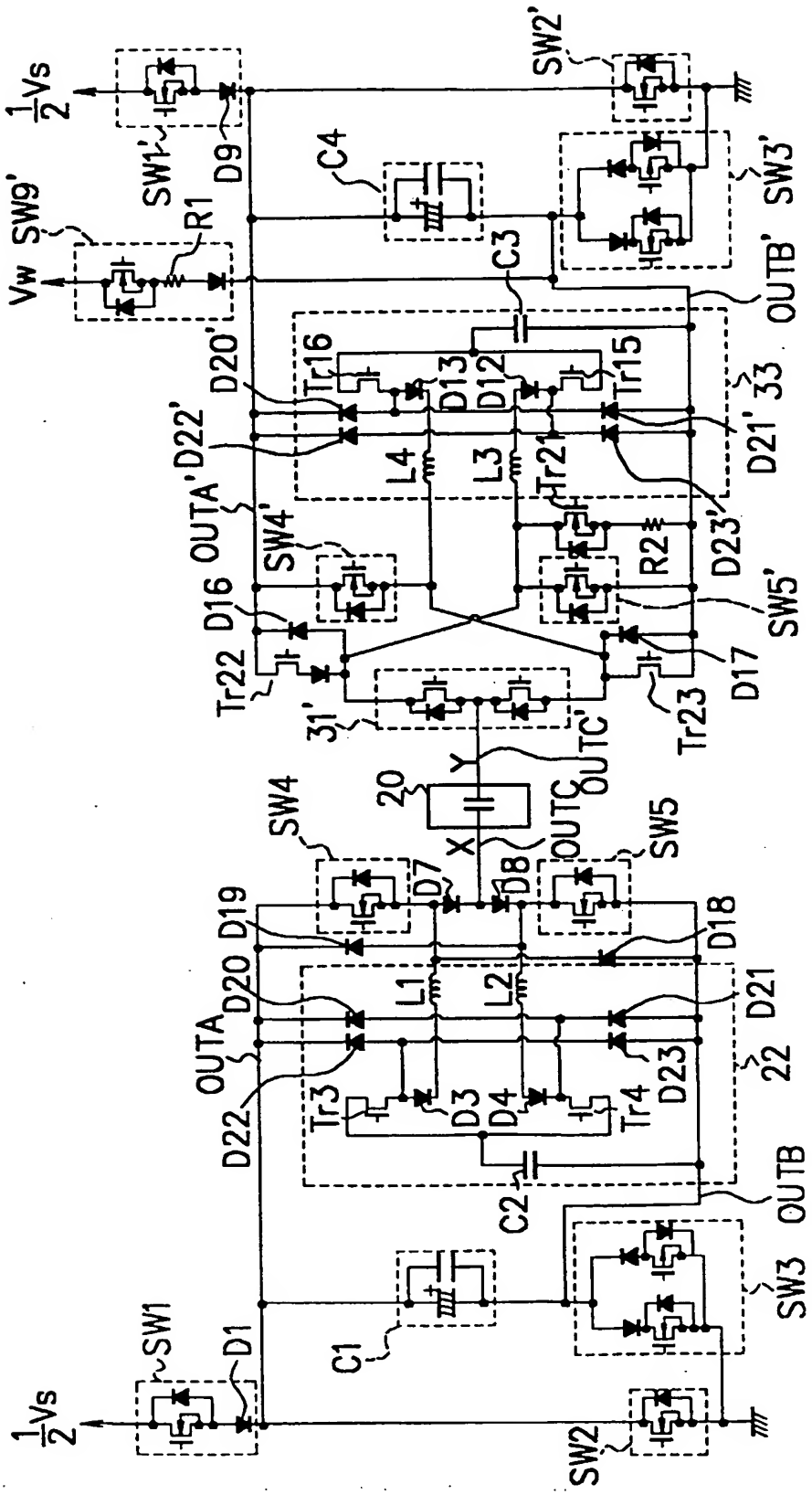

1/2Vs
SW1'
D9
SW2'
C4
SW9'
R1
Vw
C3
SW3'
OUTB'
D20'
Tr16
D13
D12
Tr15
D22'
L4
L3
Tr21
D21'
33
OUTA'
SW4'
R2
D23'
D16
SW5'
Tr22
D17
Tr23
31'
OUTC'
Y
20
X
OUTC
SW4
SW5
D7
D8
D19
D18
D20
L1
L2
D21
OUTA
22
Tr3
D3
D4
Tr4
D23
D22
C2
OUTB
SW3
SW1
D1
C1
SW2

FIG. 55

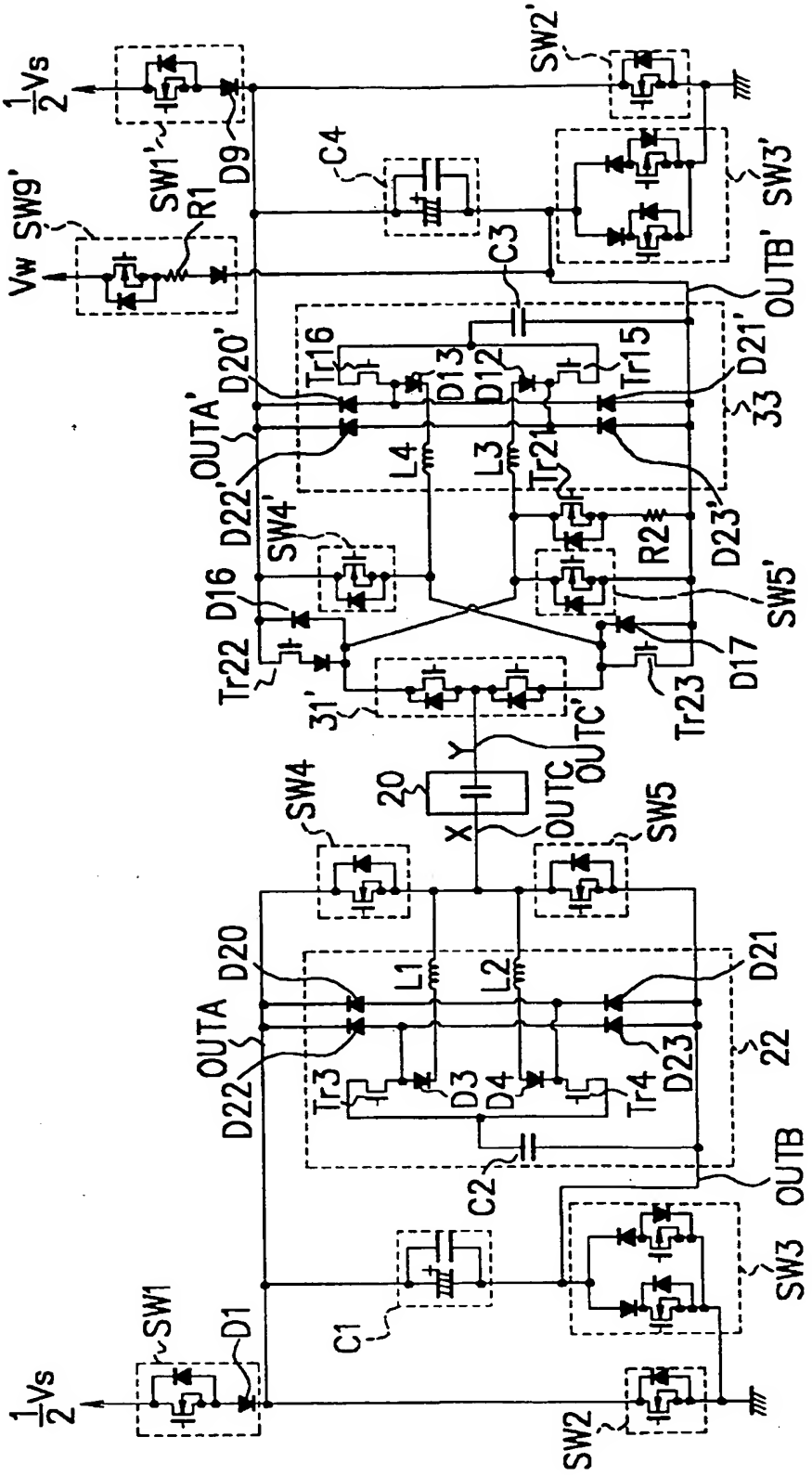

1/2Vs
SW1'
D9
SW2'
C4
SW9'
Vw
R1
C3
SW3'
OUTB'
D21'
D20'
Tr16
D13
D12
Tr15
OUTA'
L4
L3
Tr21
33
D22'
SW4'
R2
D23'
D16
SW5'
Tr22
D17
31'
Tr23
OUTC'
Y
SW4
20
X
OUTC
SW5
D20
L1
L2
D21
OUTA
D22
Tr3
D3
D4
Tr4
D23
22
C2
OUTB
SW3
C1
SW1
D1
SW2

FIG. 57

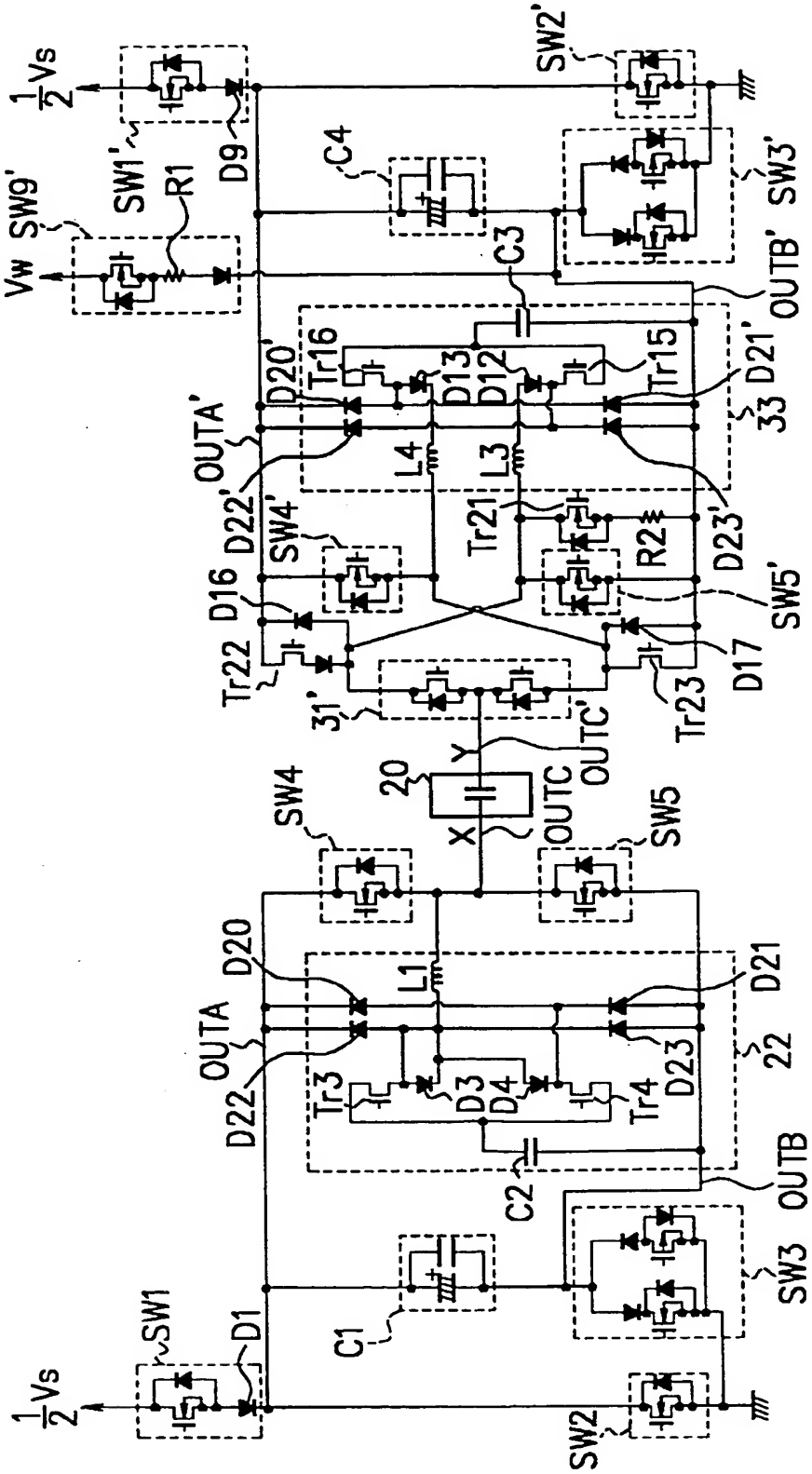

1/2Vs
SW1'
R1
D9
SW9'
Vw
C4
SW2'
SW3'
C3
OUTB'
D20'
Tr16
D13
D12
Tr15
D21'
33
OUTA'
L4
L3
D22'
SW4'
Tr21
R2
D23'
D16
SW5'
Tr22
D17
Tr23
31'
OUTC'
Y
20
X
OUTC
SW4
SW5
D20
L1
D21
OUTA
D22
Tr3
D3
D4
Tr4
D23
22
C2
OUTB
SW3
SW1
D1
C1
1/2Vs
SW2

FIG. 59

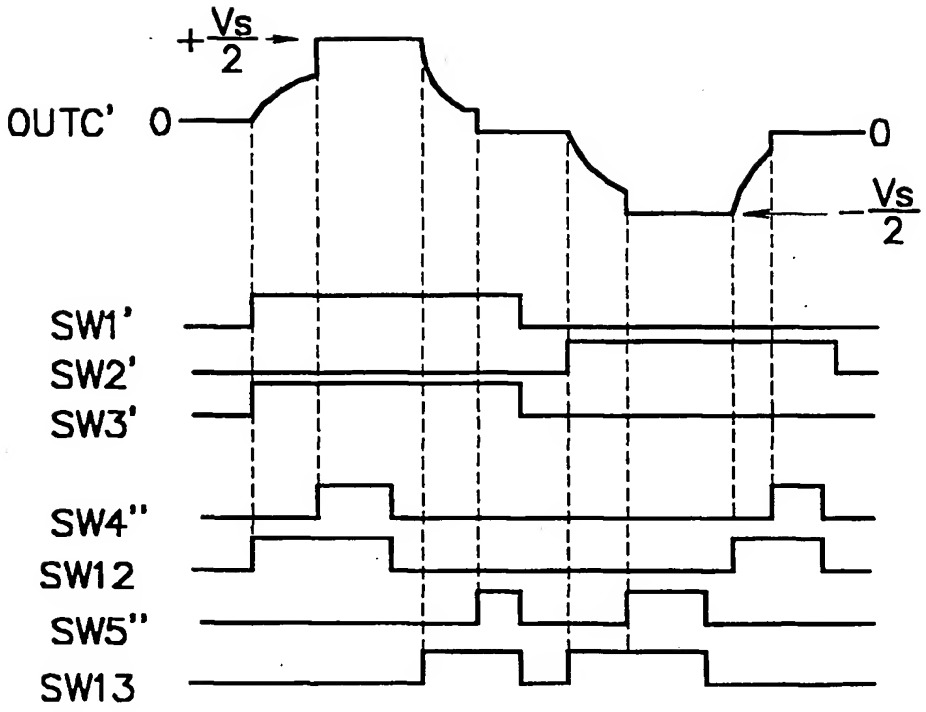


FIG. 61

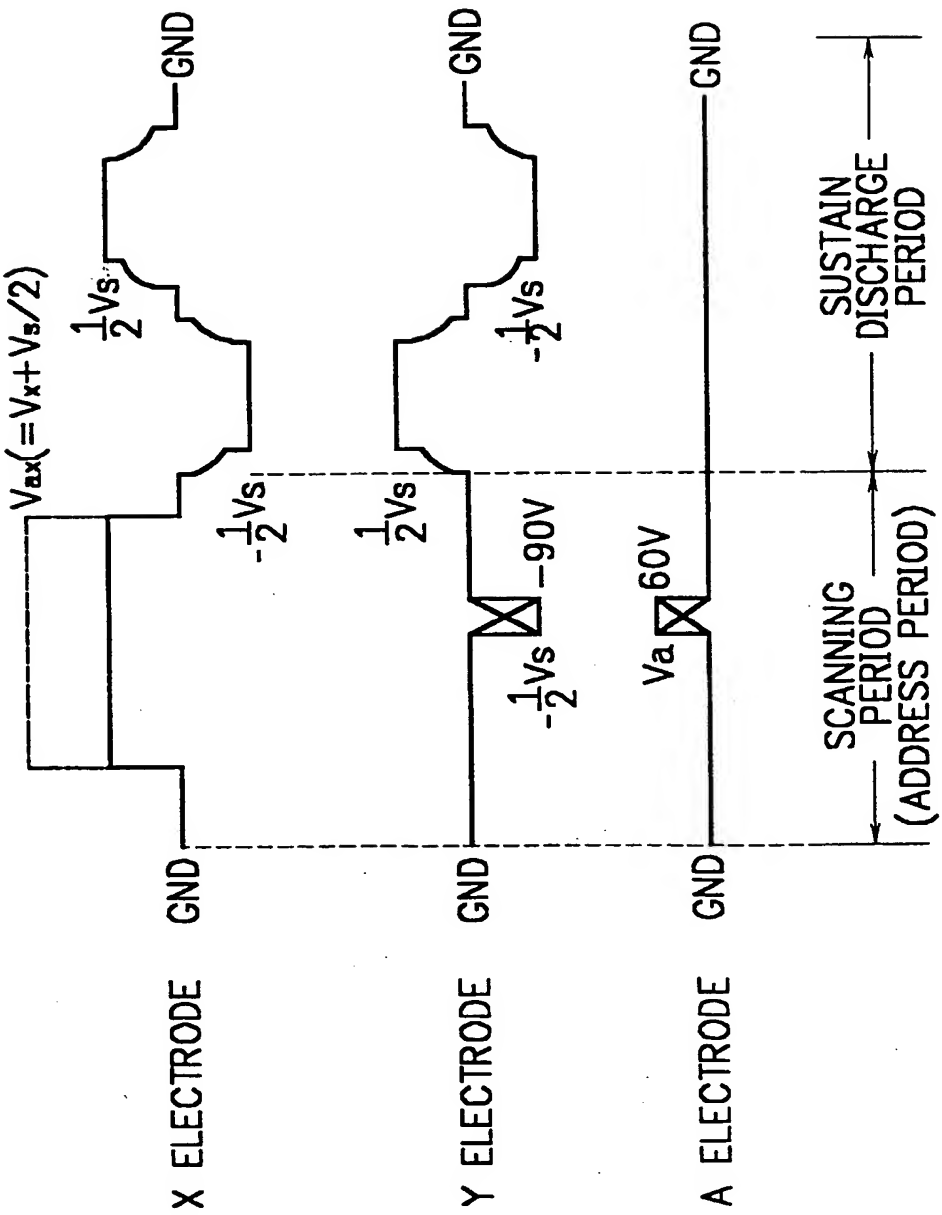

X ELECTRODE
Y ELECTRODE
A ELECTRODE
GND
GND
GND
GND
GND
GND
Vax(=Vx+Vs/2)
1/2Vs
-1/2Vs
1/2Vs
-1/2Vs
-90V
-1/2Vs
Va
60V
SUSTAIN DISCHARGE PERIOD
SCANNING PERIOD (ADDRESS PERIOD)

FIG. 63

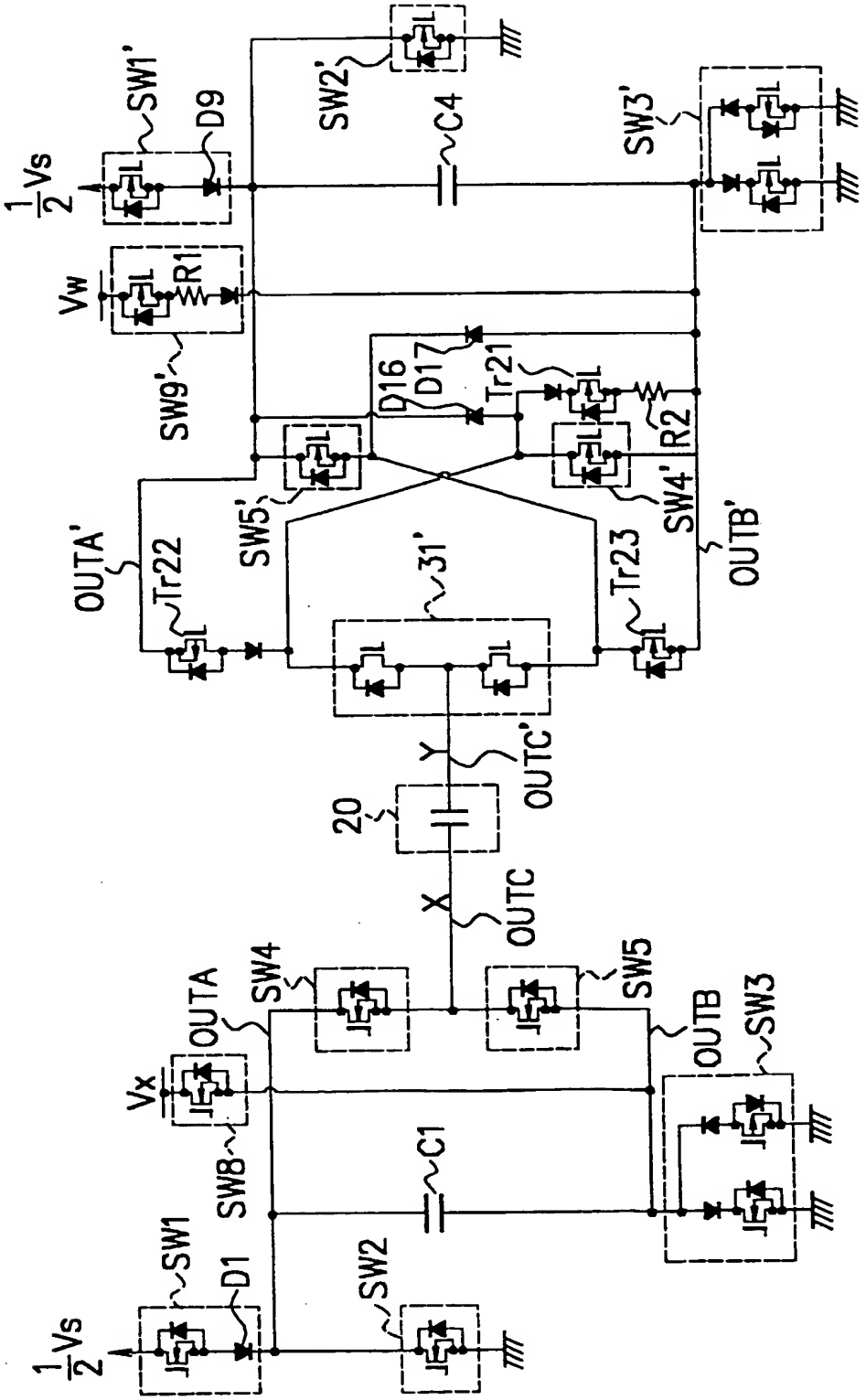

1/2Vs
SW1'
D9
SW2'
C4
SW3'
Vw
R1
SW9'
D16
D17
Tr21
R2
SW5'
SW4'
OUTA'
Tr22
31'
Tr23
OUTB'
Y
OUTC'
20
X
OUTC
SW4
SW5
OUTA
OUTB
SW3
Vx
SW8
C1
SW1
D1
SW2
1/2Vs

FIG. 65

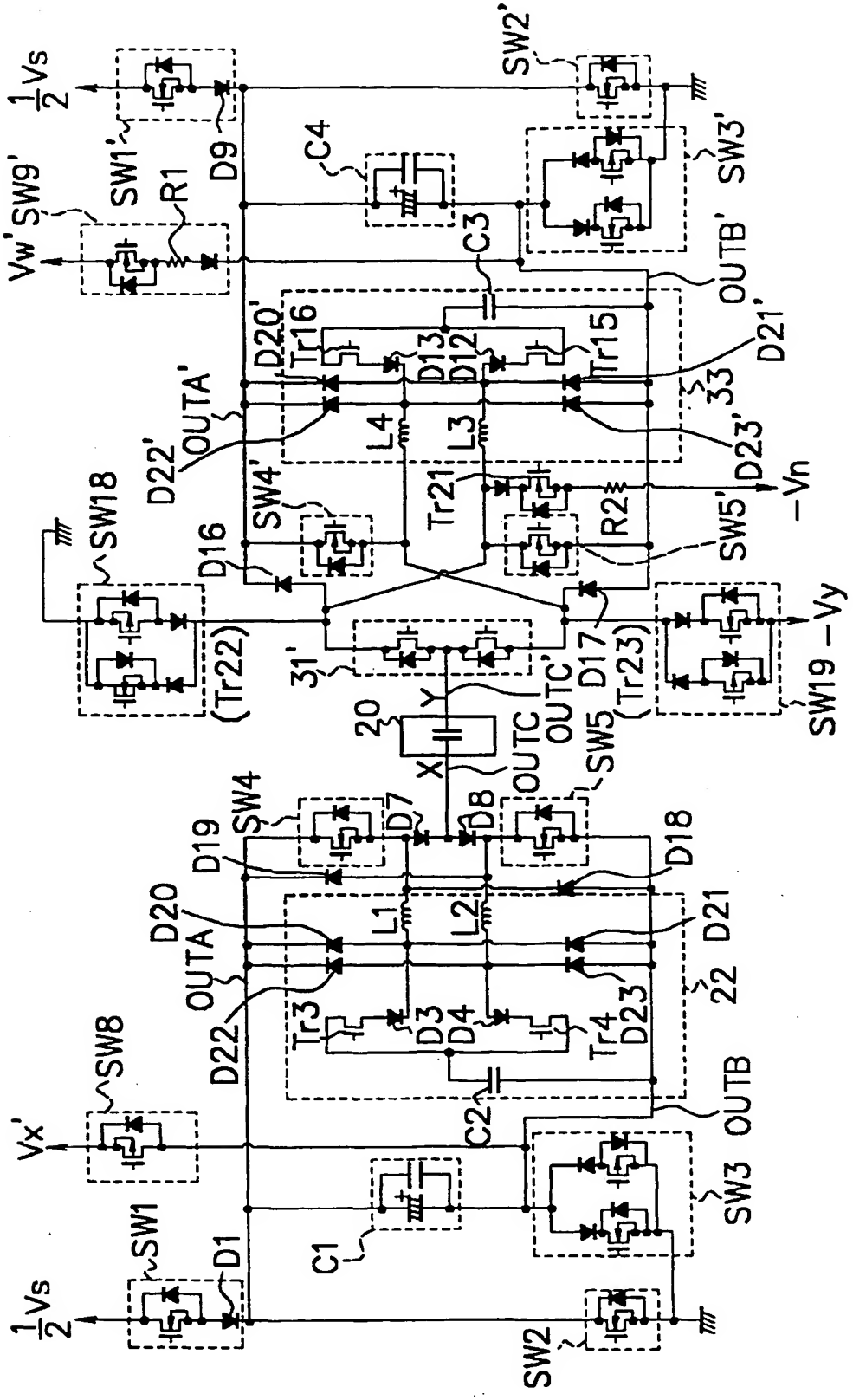

1/2Vs
SW1'
R1
D9
SW9'
Vw'
SW2'
C4
SW3'
OUTB'
C3
D20'
Tr16
D13
D12
Tr15
D21'
33
OUTA'
D22'
L4
L3
D23'
SW4'
Tr21
R2
SW5'
-Vn
SW18
D16
(Tr22)
31'
20
Y
X
OUTC'
OUTC
SW5
D17
(Tr23)
SW19
-Vy
SW4
D7
D8
D19
D18
D20
OUTA
L1
L2
D21
22
D22
Tr3
D3
D4
Tr4
D23
OUTB
SW8
Vx'
C2
SW3
SW1
D1
C1
1/2Vs
SW2

FIG. 67

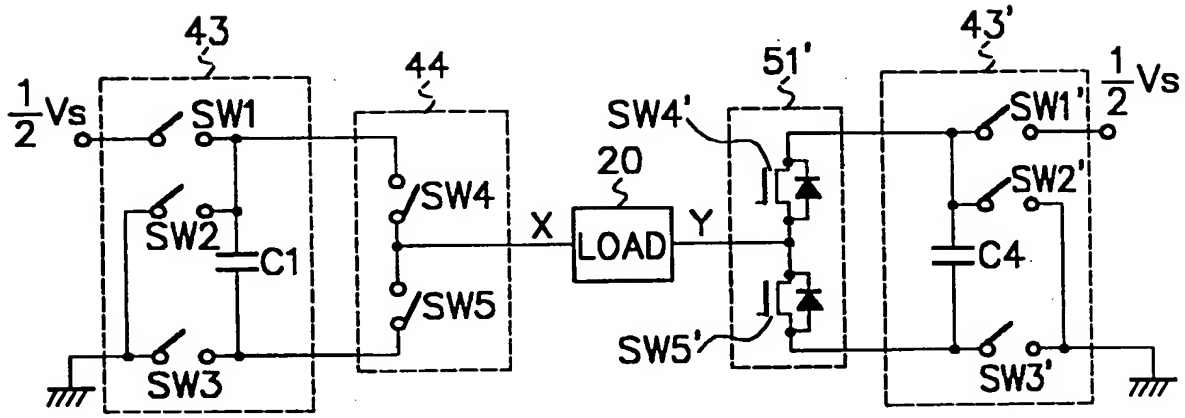

43
44
51'
43'
1/2 Vs
SW1
SW2
C1
SW3
SW4
SW5
X
20
LOAD
Y
SW4'
SW5'
SW1'
SW2'
C4
SW3'
1/2 Vs

FIG. 69

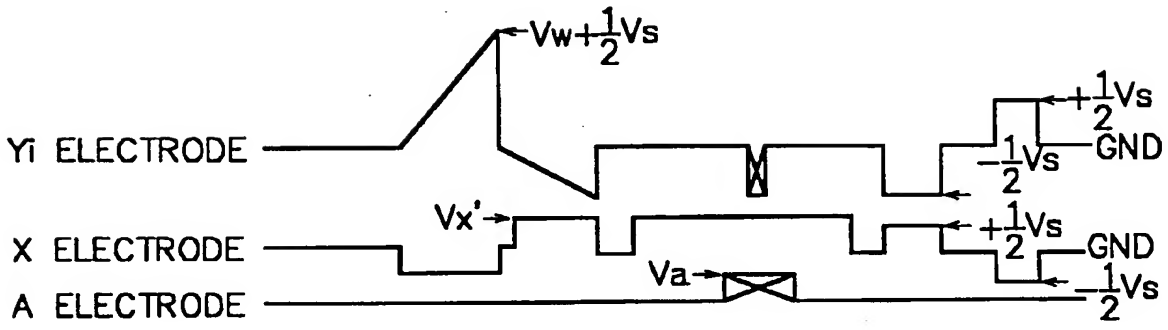

Vw+1/2Vs
Yi ELECTRODE
+1/2Vs
GND
-1/2Vs
Vx'
X ELECTRODE
+1/2Vs
GND
Va
A ELECTRODE
-1/2Vs

FIG. 71

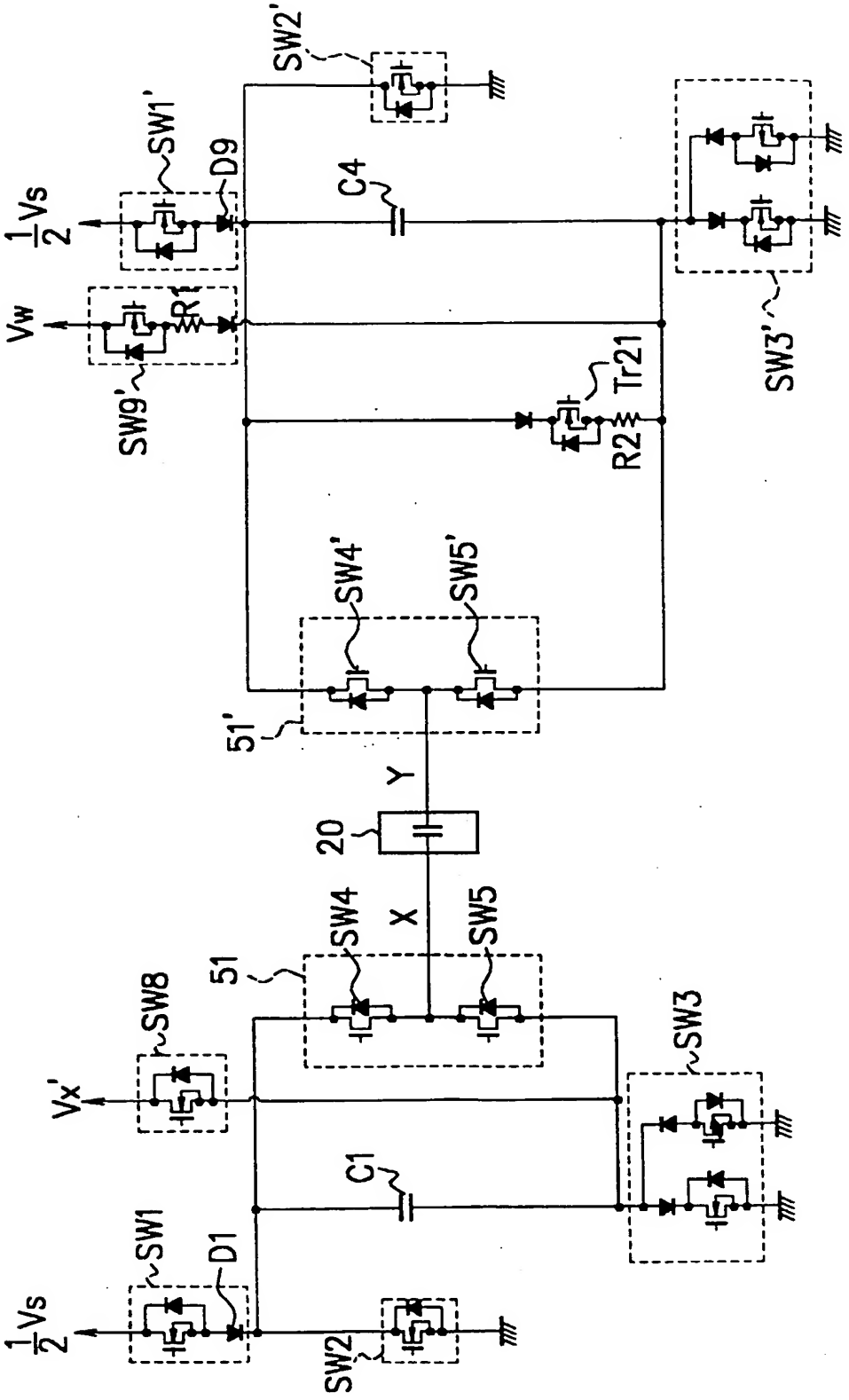

SW2'
SW1'
D9
C4
1/2 Vs
Vw
R1
SW9'
SW3'
Tr21
R2
SW4'
SW5'
51'
Y
20
SW4
X
SW5
51
SW8
SW3
Vx'
C1
SW1
D1
1/2 Vs
SW2

FIG. 73

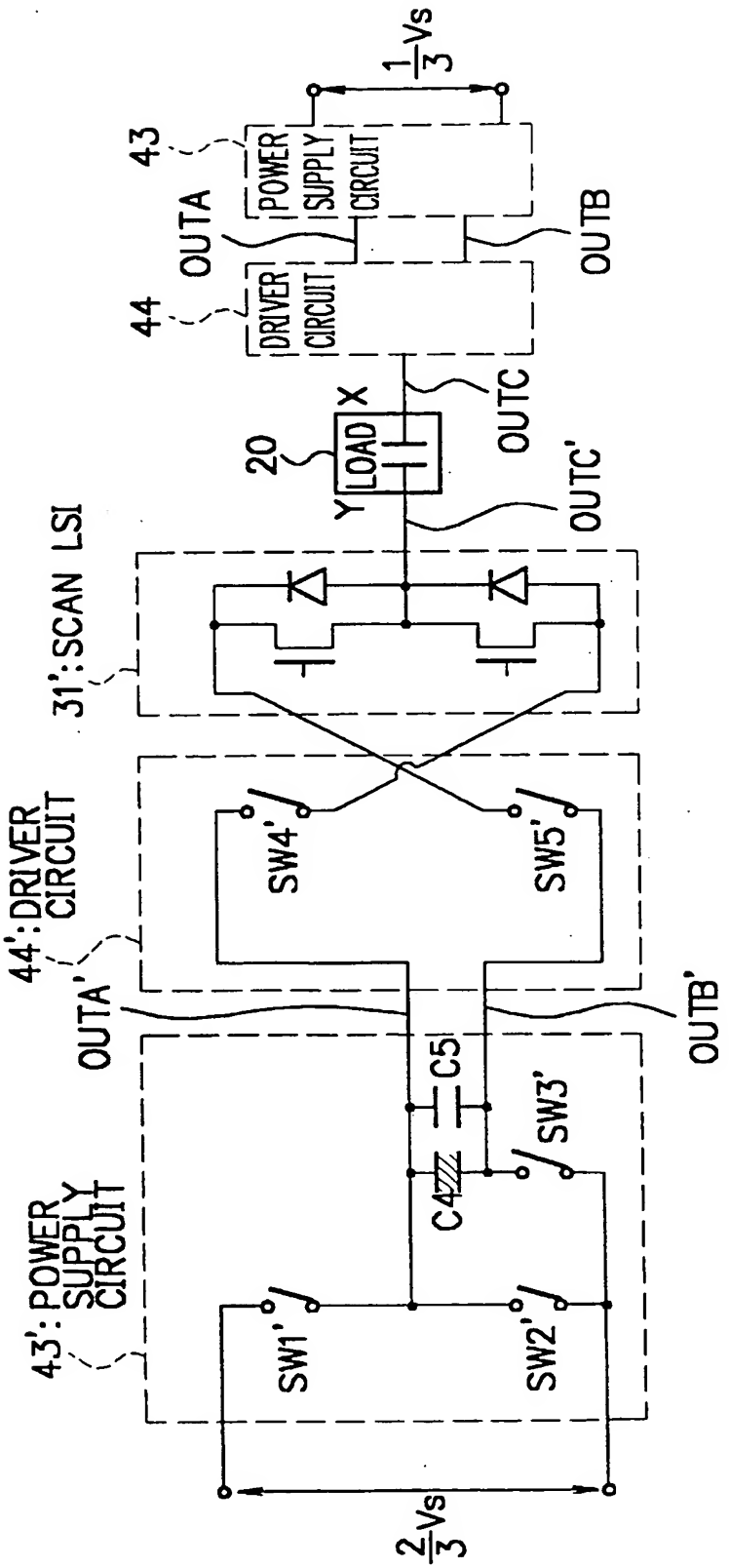

1/3 Vs
43
POWER SUPPLY CIRCUIT
OUTA
OUTB
44
DRIVER CIRCUIT
OUTC
20
X
LOAD
Y
OUTC'
31': SCAN LSI
44': DRIVER CIRCUIT
SW4'
SW5'
OUTA'
OUTB'
C5
C4
SW3'
43': POWER SUPPLY CIRCUIT
SW1'
SW2'
2/3 Vs

FIG. 75

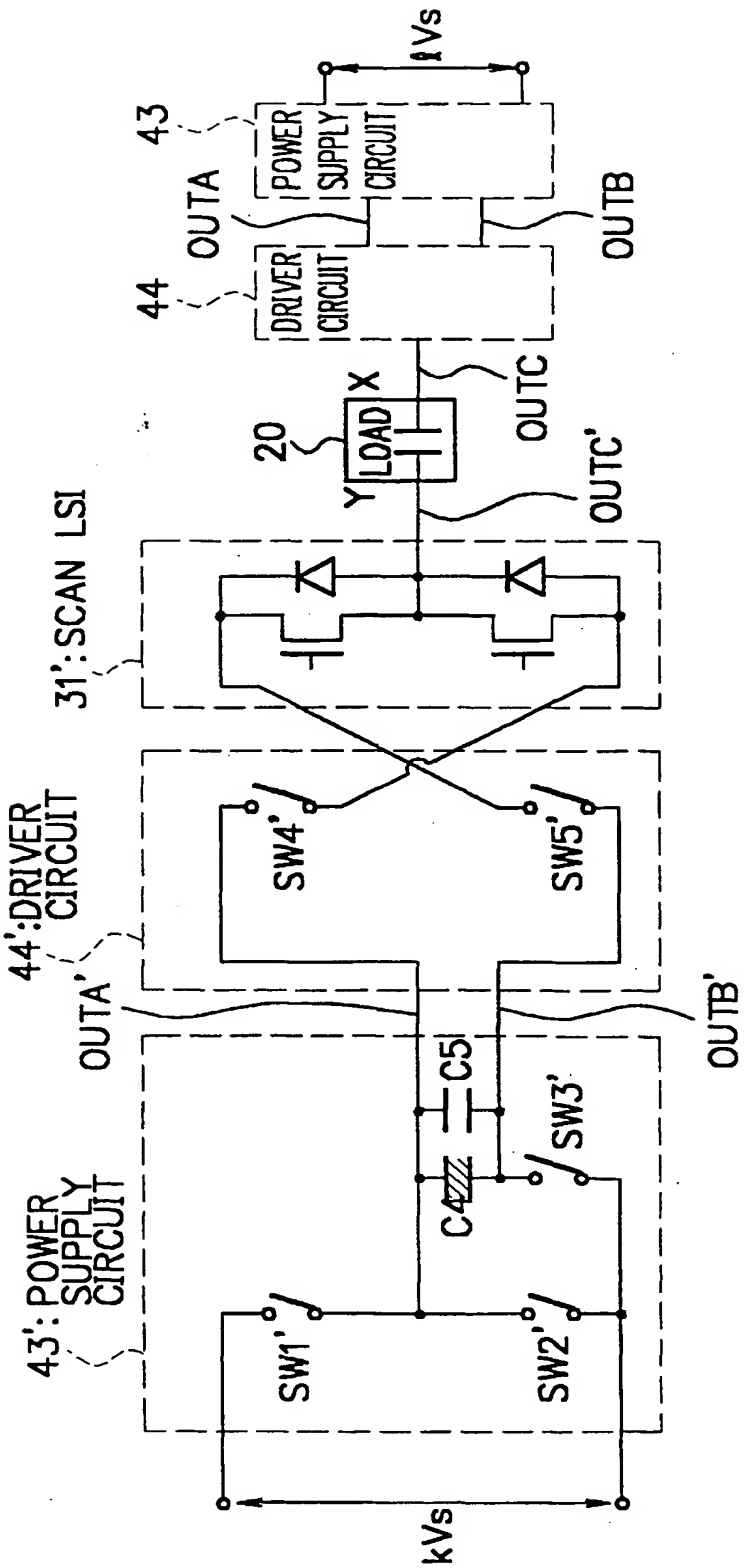

43
POWER SUPPLY CIRCUIT
Vs
OUTA
OUTB
44
DRIVER CIRCUIT
OUTC
20
X
LOAD
Y
OUTC'
31':SCAN LSI
44':DRIVER CIRCUIT
SW4'
SW5'
OUTA'
OUTB'
C5
SW3'
C4
43': POWER SUPPLY CIRCUIT
SW1'
SW2'
kVs

FIG. 77

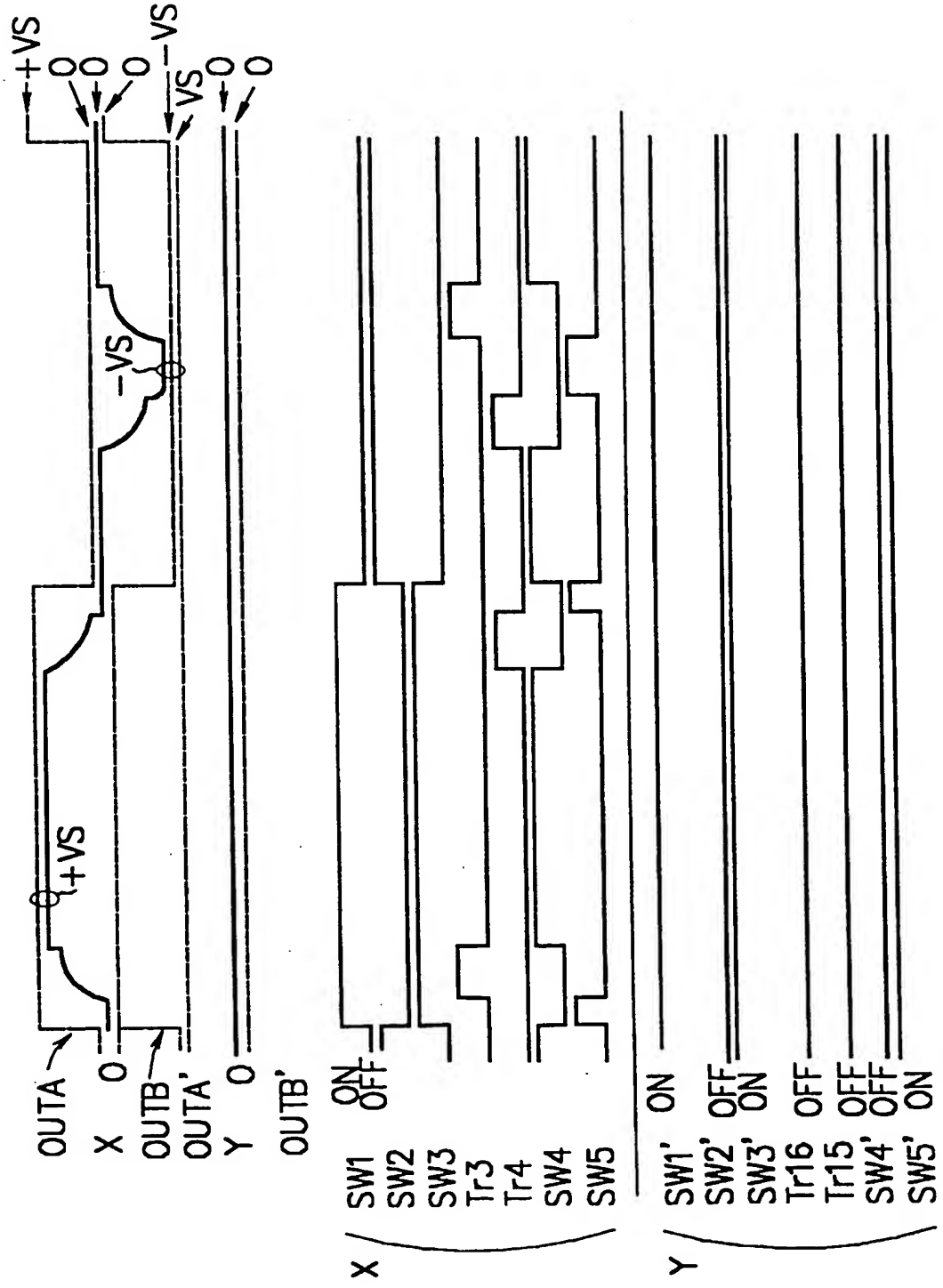

+VS
0
0
0
-VS
VS
0
0
-VS
+VS
OUTA
X
0
OUTB
OUTA'
Y
0
OUTB'
ON
OFF
SW1
SW2
SW3
Tr3
Tr4
SW4
SW5
X
ON
SW1'
SW2'
SW3'
Tr16
Tr15
SW4'
SW5'
Y
OFF
ON
OFF
OFF
OFF
OFF
ON

FIG. 79

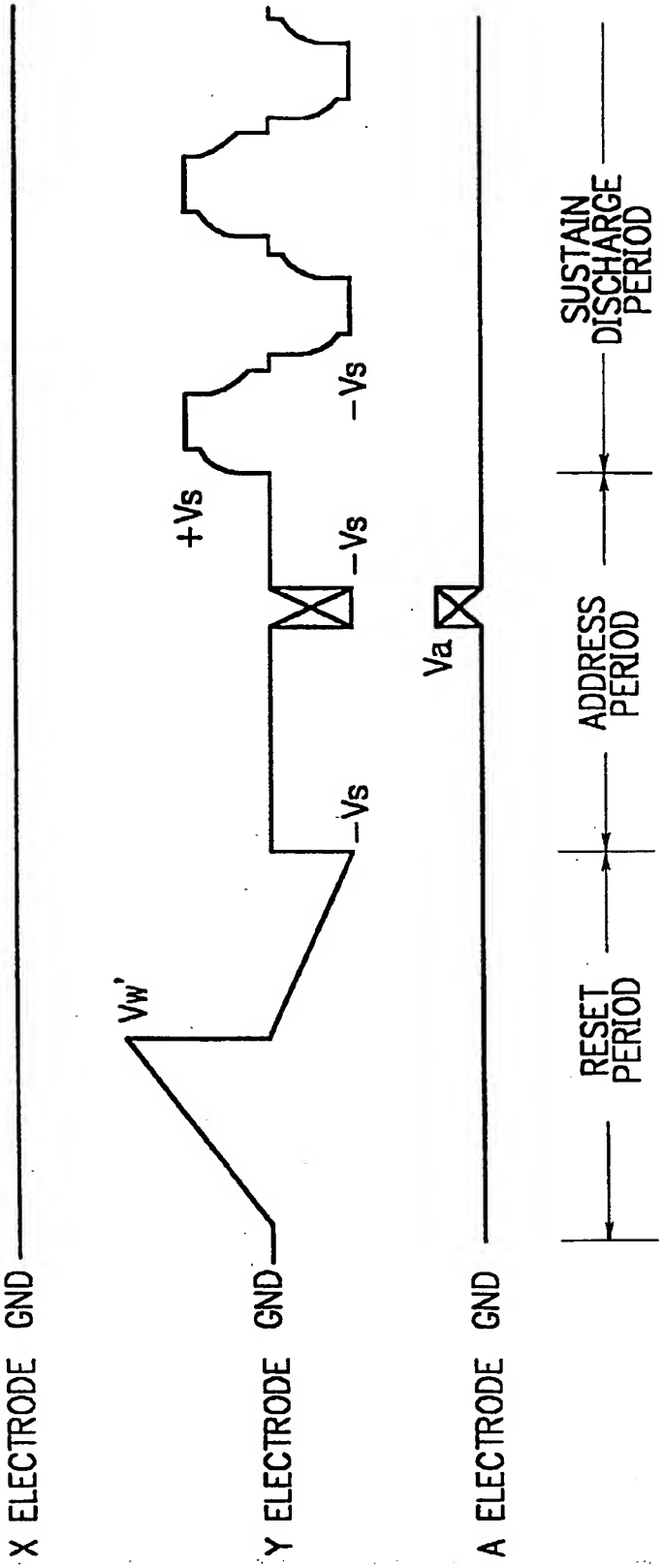

X ELECTRODE
GND
Y ELECTRODE
GND
A ELECTRODE
GND
Vw'
+Vs
-Vs
-Vs
-Vs
Va
RESET PERIOD
ADDRESS PERIOD
SUSTAIN DISCHARGE PERIOD

FIG. 81

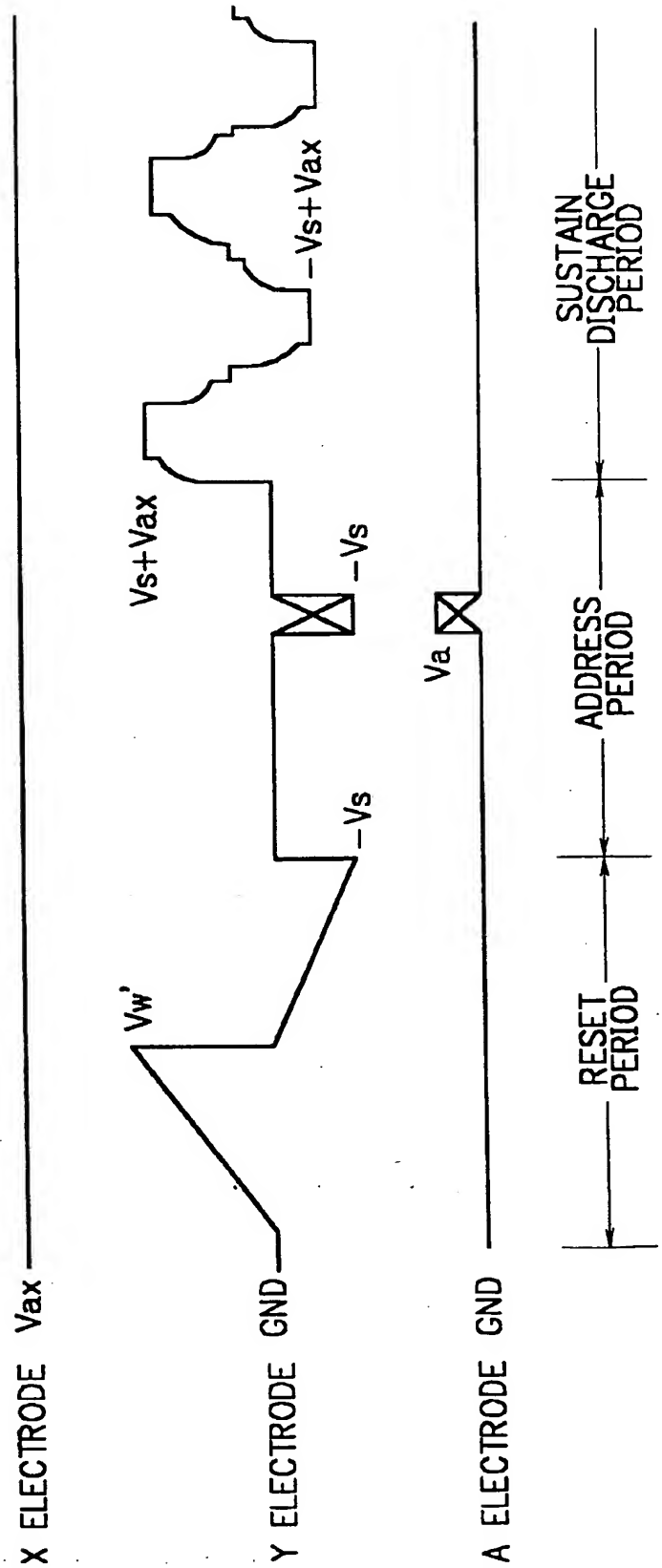

X ELECTRODE
Vax
Y ELECTRODE
GND
Vw'
Vs
Vs+Vax
Vs
Vs+Vax
A ELECTRODE
GND
Va
RESET PERIOD
ADDRESS PERIOD
SUSTAIN DISCHARGE PERIOD

FIG. 83

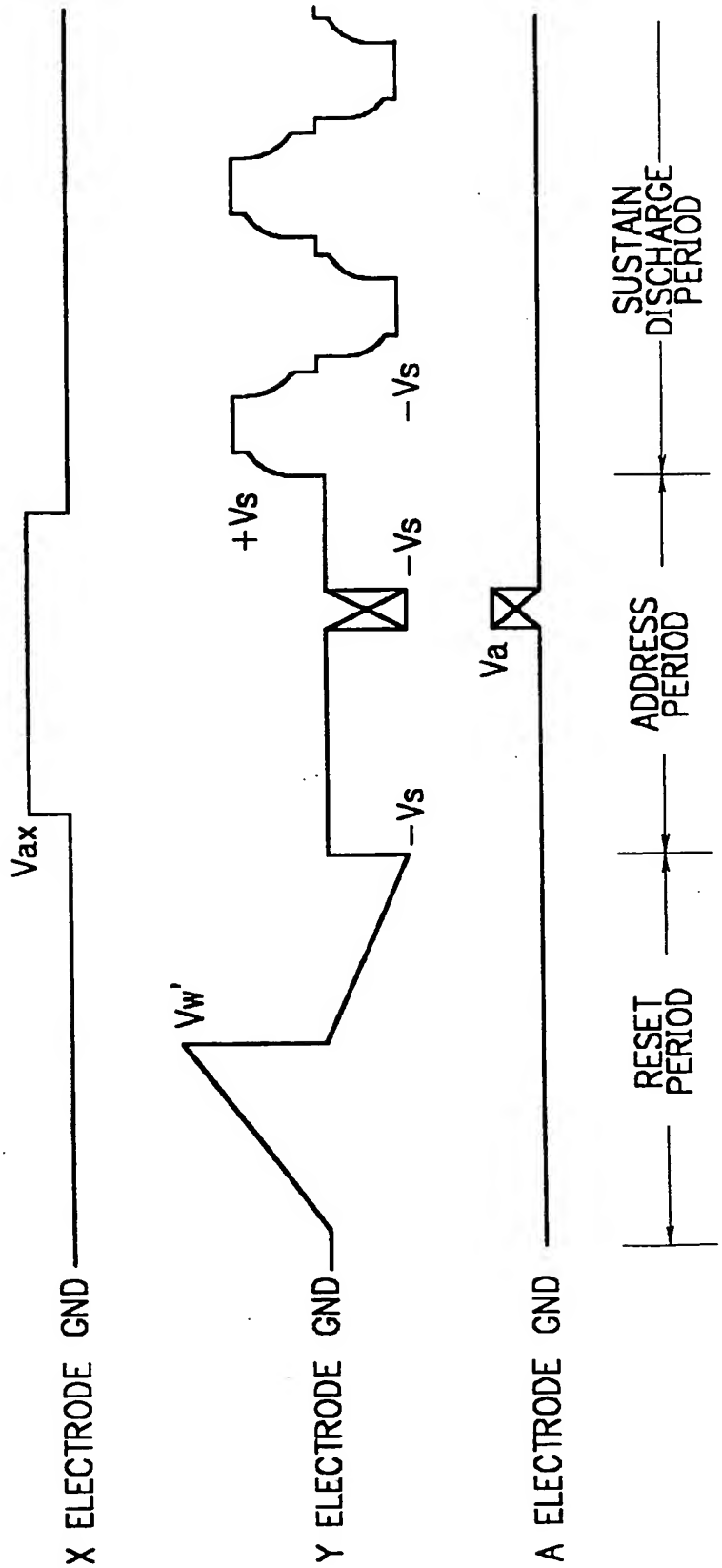

X ELECTRODE
GND
Vax
Y ELECTRODE
GND
Vw'
-Vs
+Vs
-Vs
-Vs
A ELECTRODE
GND
Va
RESET PERIOD
ADDRESS PERIOD
SUSTAIN DISCHARGE PERIOD

FIG. 85

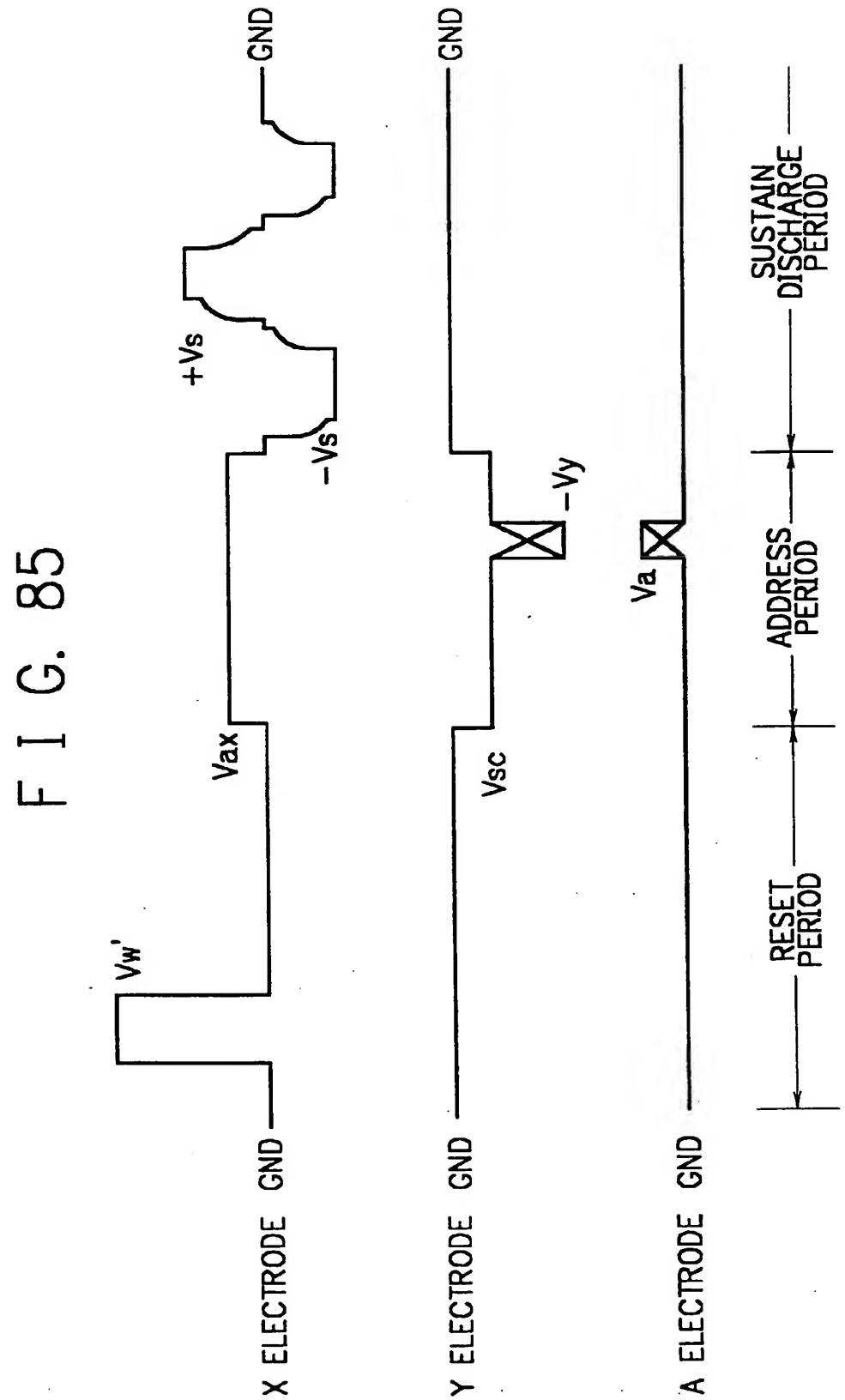

X ELECTRODE
GND
Vw'
Vax
-Vs
+Vs
GND
Y ELECTRODE
GND
Vsc
-Vy
GND
A ELECTRODE
GND
Va
RESET PERIOD
ADDRESS PERIOD
SUSTAIN DISCHARGE PERIOD

FIG. 87

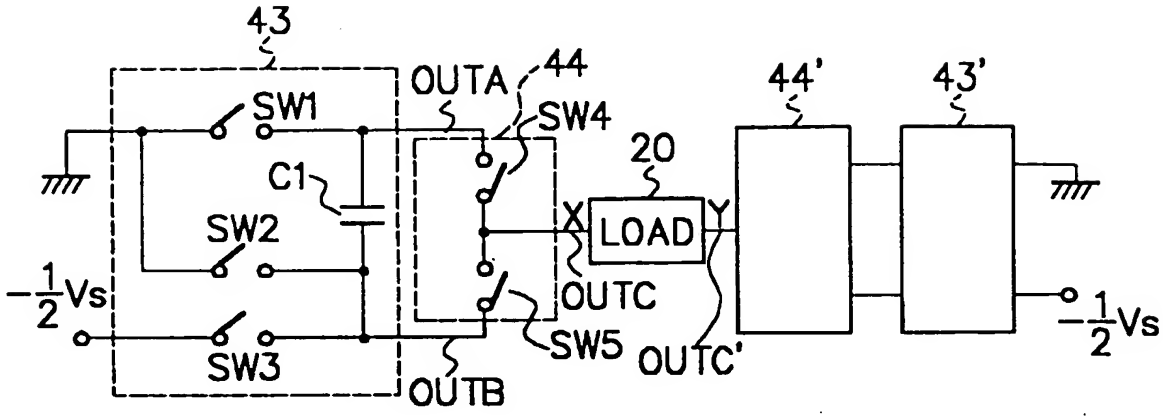

43
OUTA
44
SW1
SW4
C1
20
44'
43'
SW2
X
LOAD
Y
$-\frac{1}{2}$Vs
OUTC
$-\frac{1}{2}$Vs
SW5
OUTC'
SW3
OUTB

FIG. 88

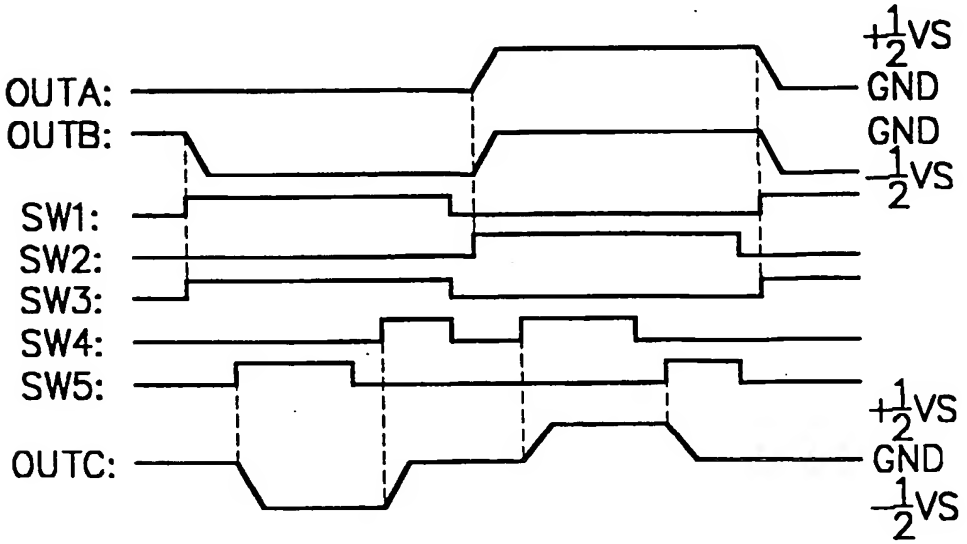

OUTA:
OUTB:
SW1:
SW2:
SW3:
SW4:
SW5:
OUTC:
$+\frac{1}{2}$VS
GND
GND
$-\frac{1}{2}$VS
$+\frac{1}{2}$VS
GND
$-\frac{1}{2}$VS

FIG. 90

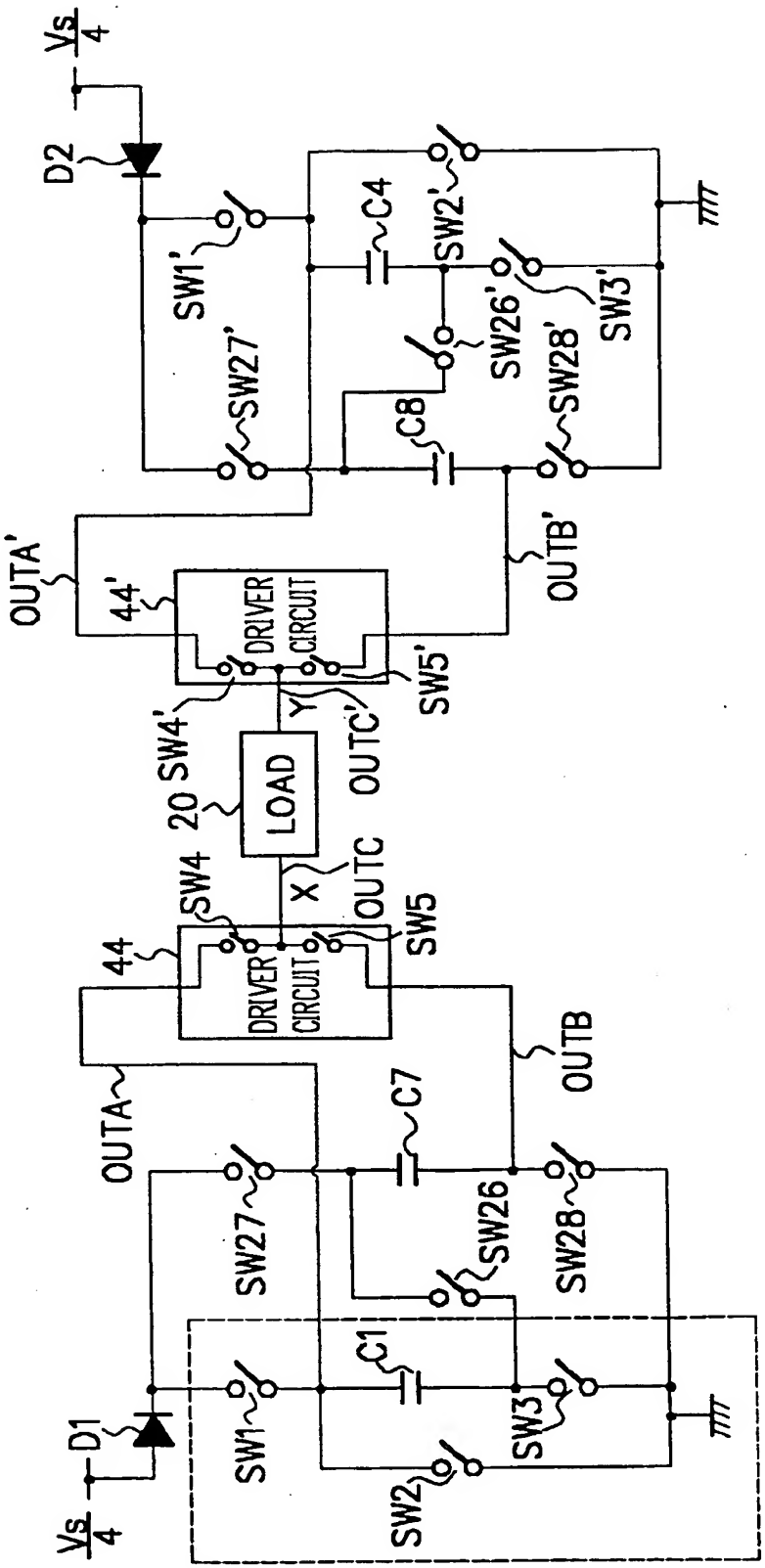

Vs/4
D2
SW1'
SW27'
C4
SW2'
SW26'
SW3'
SW28'
C8
OUTA'
44'
DRIVER CIRCUIT
SW5'
OUTB'
Y
OUTC'
SW4'
20
LOAD
SW4
X
OUTC
SW5
44
DRIVER CIRCUIT
OUTA
OUTB
C7
SW27
SW26
SW28
C1
SW1
SW3
SW2
D1
Vs/4

FIG. 92

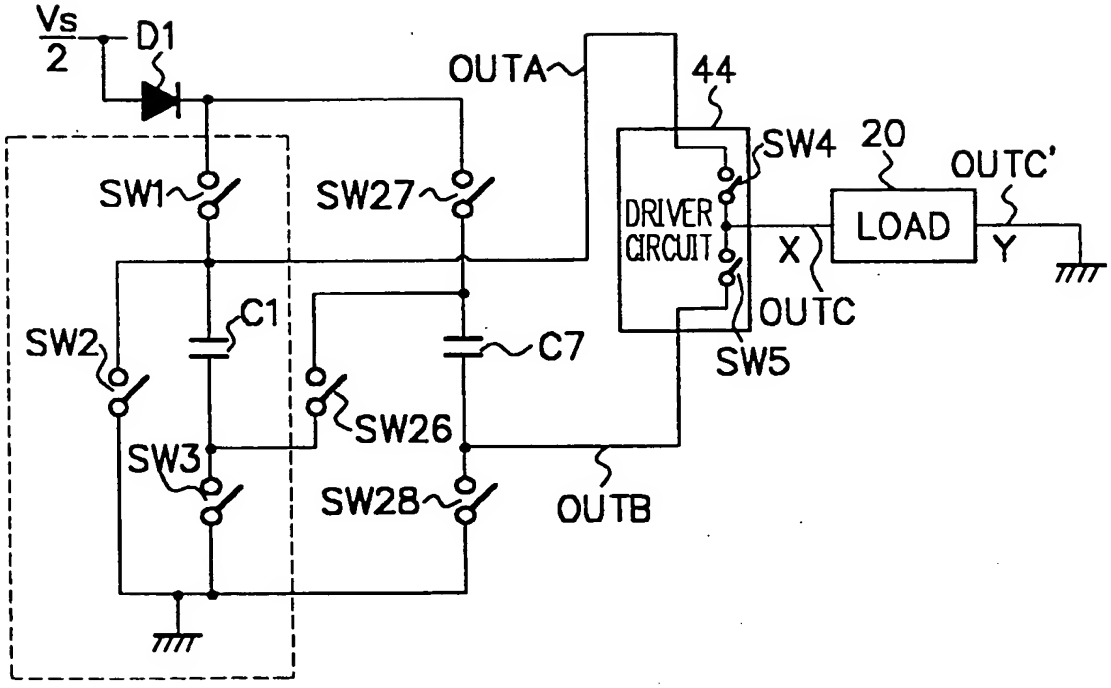

Vs
2
D1
OUTA
44
SW4
20
OUTC'
SW1
SW27
DRIVER
CIRCUIT
LOAD
X
Y
C1
SW2
C7
OUTC
SW5
SW26
SW3
SW28
OUTB

FIG. 94

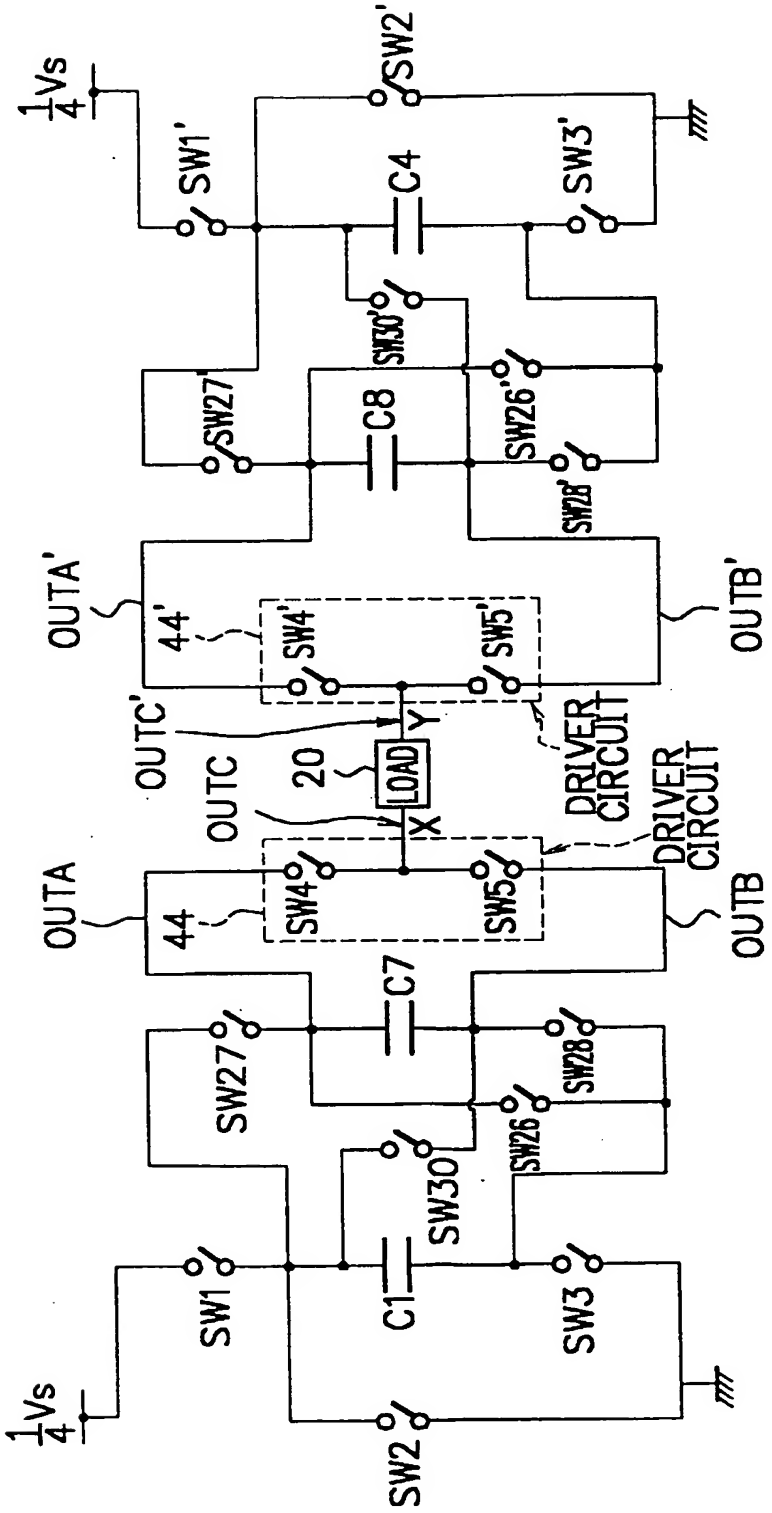

1/4Vs
SW1
SW2
SW3
C1
SW30
SW27
SW28
SW26
C7
OUTA
44
SW4
SW5
OUTB
OUTC
20
LOAD
X
Y
DRIVER CIRCUIT
OUTC'
OUTA'
44'
SW4'
SW5'
OUTB'
C8
SW30'
SW27'
SW28'
SW26'
SW1'
SW2'
SW3'
C4

FIG. 96

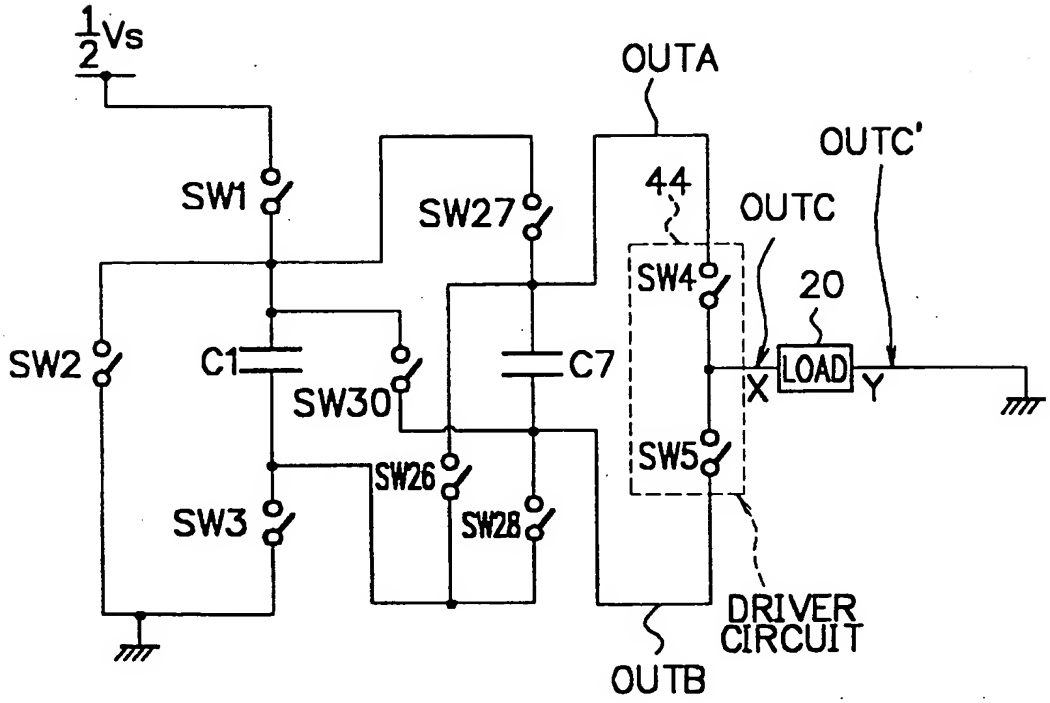

1/2Vs
OUTA
OUTC'
SW1
SW27
44
OUTC
SW4
20
SW2
C1
SW30
C7
LOAD
X
Y
SW5
SW26
SW3
SW28
DRIVER CIRCUIT
OUTB

FIG. 98

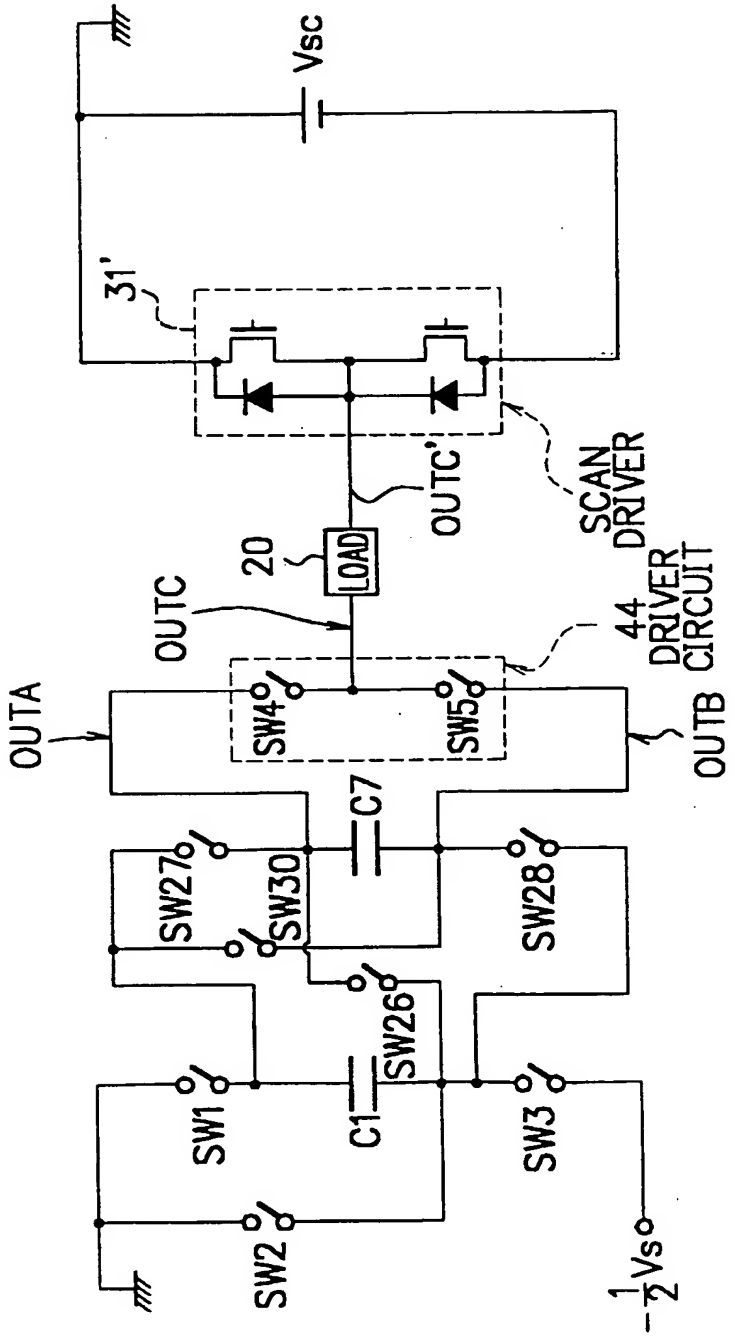
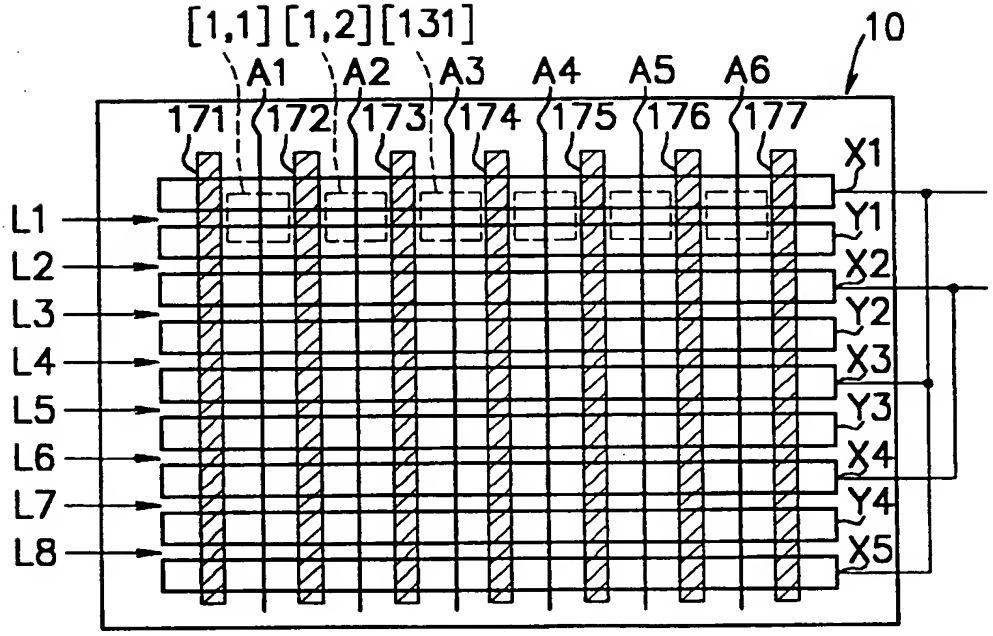

Vsc
31'
SCAN DRIVER
OUTC'
20
LOAD
OUTC
44
DRIVER CIRCUIT
OUTA
SW4
SW5
OUTB
C7
SW27
SW30
SW28
SW26
SW1
C1
SW3
SW2
$-\frac{1}{2}$Vs

FIG. 100



10: PDP
X1~X5: ELECTRODE X
Y1~Y4: ELECTRODE Y
A1~A6: ADDRESS ELECTRODE
L1~L8: DISPLAY LINE
171~177: PARTITION

F I G. 102

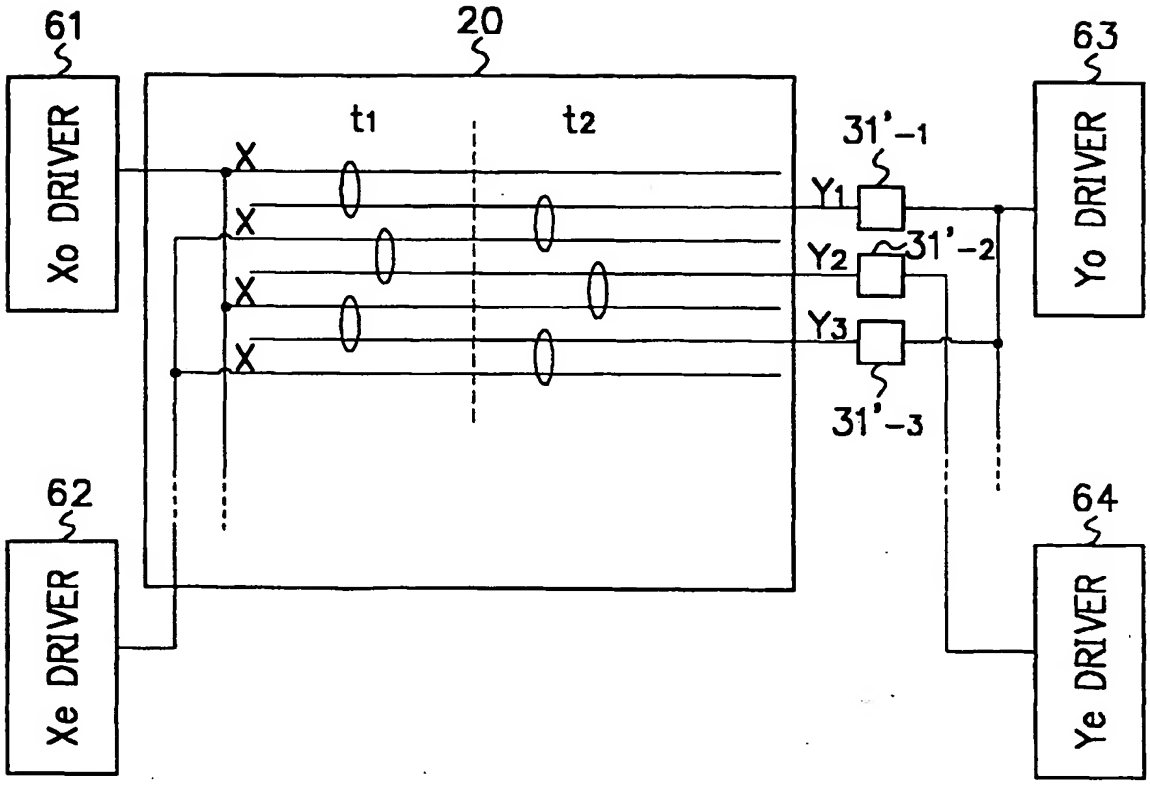

61
20
63
Xo DRIVER
t1
t2
31'-1
Y1
Y2
31'-2
Y3
31'-3
Yo DRIVER
62
64
Xe DRIVER
Ye DRIVER

FIG. 104